

THE DIGITAL GROUP

C A S S E T T E S T O R A G E S Y S T E M

CSSB-0-RØ

the digital group

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I. INTRODUCTION

The Digital Group Cassette Storage System is a total magnetic tape data storage and retrieval system capable of controlling up to four Phi-Deck cassette transports and accessing any of over one million 8-bit bytes within 20 seconds, using standard C-30 Phillips cassettes.

The system is ideal for general purpose data and program storage, file copying, editing, and sorting operations. Each deck is fully controlled to prevent tape breakage. Electronic braking precisely controls tapes for fast forward and rewind operations. A 4- to 5-bit translation scheme called Group Coded Recording, allows higher packing densities with a soft error rate of less than one bit in 10^8 . This system operates at 1600 flux changes per inch, yielding a data transfer rate of 800 bytes per second at a tape speed of five inches per second.

SPECIFICATIONS

Recording Density: 1600 FCPI (Flux Changes Per Inch)

Data Density: 1280 BPI (Bits Per Inch)
using 4- to 5-bit Group Coded Recording

Data Rate: 800 Bytes per second (6400 Baud)

Data Capacity: 250,000 bytes on each side of a C-30 audio cassette
540,000 bytes on each side of 300 foot data cassette

Tape Speed: 5 IPS Read/Write
100 IPS Fast Forward/Reverse

Speed Tolerance: $\pm 20\%$ (i.e., the system will read a tape that was recorded 20% from the nominal speed without adjustment. It will read tapes outside this range by adjusting the data rate control.)

Error Rate: Soft - less than 1 bit in 10^8
Hard - virtually zero when using the software package supplied with the system and a good quality audio tape

Power: +5V DC $\pm 5\%$
1.0 Amps nominal 1 drive
2.0 Amps maximum 4 drives
4.0 Amps peak for .1 second during drive enable

+12V DC unregulated (limits: 11V-20V)
0.4 Amp average with tape moving
0.7 Amp peak during motor start

II. SOFTWARE INTERFACE

Since the absolute method of controlling the cassette system will differ for each installation, only a basic interface will be described. The user can then modify the basic interface to meet his own requirements.

COMMANDS

The command port (see Table 2.1) interprets the various commands into tape motion and activates the read/write electronics. The two select bits, SEL1 and SEL2, select the active deck, according to Table 2.2. The selected deck can only be changed when all decks are stopped (status bit NOT BUSY is on). Otherwise, even though a command may specify a different deck, the original deck will be used. ENABLE/DISABLE (Enable=1, Disable=0) controls the deck capstan motors so that they may be turned off under software control. The capstan motors should be enabled during and at least one second prior to any other commands. STOP/RUN (Stop=1, Run=0) controls tape motion. The STOP command also takes up slack in the tape. FWD/REV (Fwd=1, Rev=0) controls tape direction, and SLOW/FAST (Slow=1, Fast=0) controls tape speed. Note that since "slow reverse" cannot be performed, a "slow forward" is automatically substituted. RCD/READ (Record=1, Read=0) controls the Read/Write electronics, and ERASE (=1) will erase the tape when RCD is selected. All commands other than the RECORD or ERASE commands should have RCD/READ=0 to prevent recording spurious glitches on the tape.

Table 2.1

Status and Command Ports

<u>COMMAND PORT</u>			<u>STATUS PORT</u>	
<u>Bit</u>	<u>Definition (1 active)</u>		<u>Bit</u>	<u>Definition (1 active)</u>
0	SEL 1		0	OVERRUN/UNDERRUN
1	SEL 2		1	READY (data ready or ready for data)
2	1=ERASE		2	STOP (possible jam or end of tape)
3	1=RECORD	0=READ	3	NOT BUSY (user may change decks)
4	1=STOP	0=RUN		
5	1=FORWARD	0=REVERSE		
6	1=SLOW	0=FAST		
7	1=ENABLE	0=DISABLE		

Table 2.2

Deck Selection

	<u>SEL 2</u>	<u>SEL 1</u>	<u>DECK</u>
	0	0	0
	0	1	1
	1	0	2
	1	1	3

STATUS

The status port (see Table 2.1) provides information on the state of the controller. Four status bits are brought out, leaving four input bits for other uses. Two of the bits, STOP and NOT BUSY, supply information on the deck status. STOP is an immediate response to a stop command or a jam. NOT BUSY occurs about a second after STOP turns on, signifying the deck is totally stopped. STOP is used by the software in all cases, except to switch the selected deck, which can only occur in a not busy state. The other two bits are status bits for the read/write electronics. READY indicates that the deck can accept another data byte (in Record) or that a new data byte is in the DATA-OUT port (in Read). READY is reset about one millisecond after it is set. It is also reset by a command, data in, or data out strobe. OVERRUN/UNDERRUN indicates that the computer has not serviced a READY by supplying or looking at the new character within the required time. It will remain set until a new command is issued. It is to be treated in most cases as an error condition.

INPUT DATA (FOR RECORD)

The data input port requests the data bytes which are to be recorded on the tape. The first byte should be loaded either prior to issuing the record command or within about five milliseconds after issuing the record command. Each subsequent byte of data to be recorded should be loaded when the READY status goes high. Loading the new byte will automatically reset the READY line. The byte should be loaded within .5 milliseconds after the READY signal. Otherwise, OVERRUN/UNDERRUN will come on, and the record electronics will go into erase mode. This may be allowed to happen at the end of a data block in order to record an inter-record gap. If a new command is to be given immediately after the last recorded byte, the OVERRUN/UNDERRUN bit must come on before the command is given. If the command is issued earlier, part of the last byte will not be recorded.

OUTPUT DATA (FOR READ)

The data output port is loaded by the read/write electronics with the data being read from the tape. After issuing a read command, the electronics will look for a sync pattern and then load the output port with the first data byte. At this time, READY will go high. When the byte is read, the READY signal will be reset. The byte should be read within .5 milliseconds after the READY signal. Otherwise, OVERRUN/UNDERRUN will come on, and the read electronics will be halted until another read command is issued.

MECHANICAL CONSIDERATIONS

Since the various tape and head movements require certain amounts of time to stabilize, consideration must be given by the software to insure error free read and record operations.

1. Never issue a record command (or turn on the record bit) when the tape is in any state other than slow forward, and the tape is stabilized against the head. The tape may take as much as one second to align itself with the tape guides on the head and an unaligned tape may record errors. A good practice to insure reliable recording is to read the previous block without error. This implies the tape is tracking correctly for the record operation.
2. When issuing a read command which causes the head to come up against the tape, noise and random patterns as the tape becomes aligned may cause false synchronizing and give erroneous read data. Therefore, it is a good practice in this situation to wait about a second, and then reissue the read command, using only the data from this second read command.
3. When recording the first block of data at the start of a tape, issue an erase command, and then time out about five to seven seconds to allow the tape leader to pass before recording data.
4. To allow the recording of two consecutive blocks at different points in time, always go into erase mode after recording the first block for a time longer than the space between blocks. (This is easily done by ignoring the READY after the last byte has been recorded, and timing out for the erase time. The electronics will immediately begin erasing without glitching) When the next block is to be recorded, it is begun somewhere within the erased section, thus preventing any glitching and subsequent false synchronizing on read operations.

The following bit patterns are recommended for issuing the various commands:

COMMAND	Bit:	ENABLE	SLOW FAST	FWD BKW	STOP RUN	RECORD READ	ERASE	
		7	6	5	4	3	2	1
36- STOP		1	1	1	1	0	0	Selected Deck
24- FAST FORWARD		1	0	1	0	0	0	(Note: Sel-
20- FAST REVERSE		1	0	0	0	0	0	ected deck may
34- READ		1	1	1	0	0	0	only be changed
35- RECORD		1	1	1	0	1	0	when status bit
35(4+)- ERASE		1	1	1	0	1	1	NOT BUSY is on.)
16- STANDBY		0	1	1	1	0	0	

III. HARDWARE INTERFACE

Computer Interface

The basic interface of the cassette controller to the computer occurs through four controller I/O ports. These ports may be connected in various schemes to fully utilize the hardware arrangement of the computer.

The computer's output ports connect to the command port and the data-in port. The computer's input ports interface to the data-out port and the status port. Each port has its own strobe line which is used either to strobe information into the internal latch or to activate the tri-state output in order to read the port.

All outputs from the controller will support ten TTL loads, and all data or control inputs are one TTL load. The command strobe is two TTL loads, the data-in strobe is three TTL loads, the status strobe is four TTL loads, and the data-out strobe is five TTL loads. The data-out and status ports are tri-state, activated by their respective strobes. All strobe signals are active low, and should remain high when not in use. The command data-in and data-out strobes should be low for a period greater than 500nsec, but less than one millisecond. A strobe greater than one millisecond is likely to cause false status indication from the read/write electronics.

Some typical connections are shown below. Figure 3.1 depicts a setup where all input and output ports are provided by the computer. Unless all strobes are obtainable from the computer, a third output port will have to be dedicated for software controlled strobe pulses. The scheme in Figure 3.2 uses this strobe port, but takes advantage of a bus system, since the strobes are no longer tied to specific ports but are under software control. Figure 3.3 uses a bus system found on more complex systems. Here, inputs and outputs are shared on the same line and controlled totally by the strobe signals. Care should be taken when using this method not to load the bus beyond its capacity.

Deck Interface

The cassette controller must also be interfaced to the decks. Refer to Figure 5.1 for the wiring of the decks. The board has four separate connections for each of four decks on all pins except ALLCAP, CAPSUPPLY, ALLENGSW, and ALLENGSWGND. The connectors supplied with the deck cables (when decks are included with the controller) will plug into connections for decks 0 and 1. When decks 2 and/or 3 are used, the above signals must be wired into the connector for deck 0 or 1. Also, HDGND is a common head ground, and all cable shields must be terminated at these two pins.

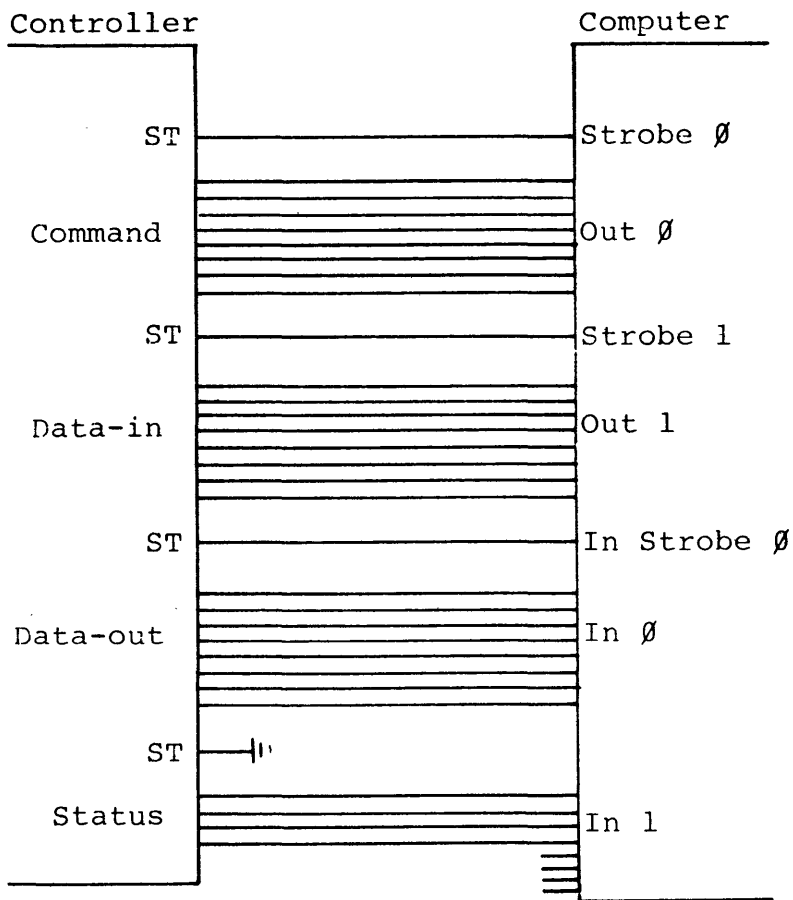


Figure 3.1 Dedicated I/O Ports

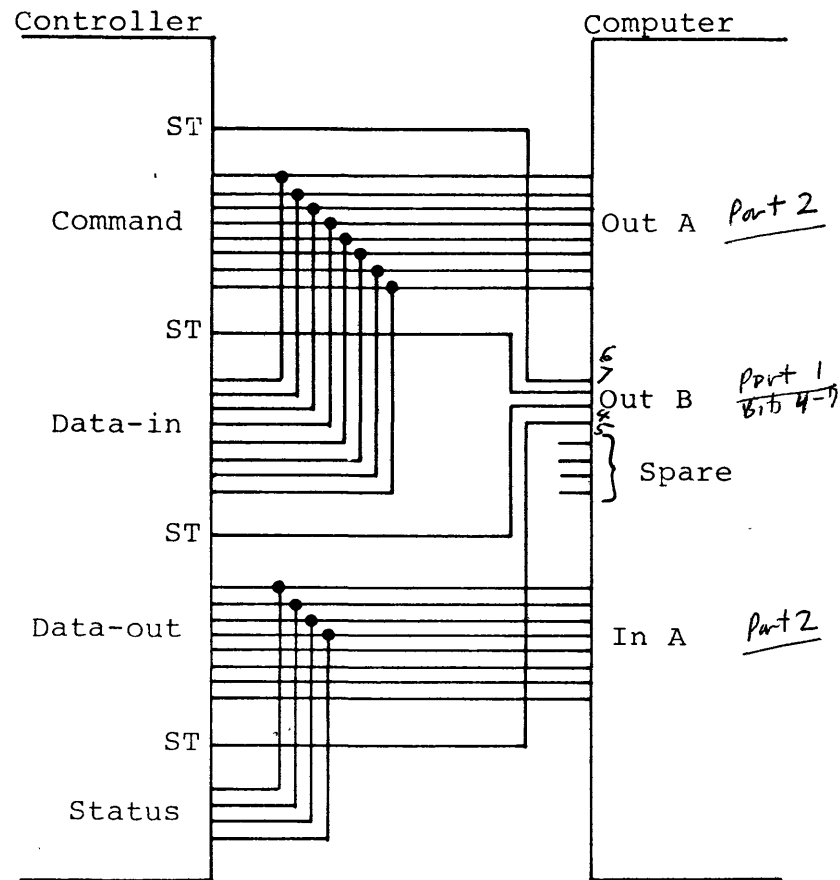


Figure 3.2 Multiplexed I/O Ports with Dedicated Strobes (Used with Digital Group Systems)

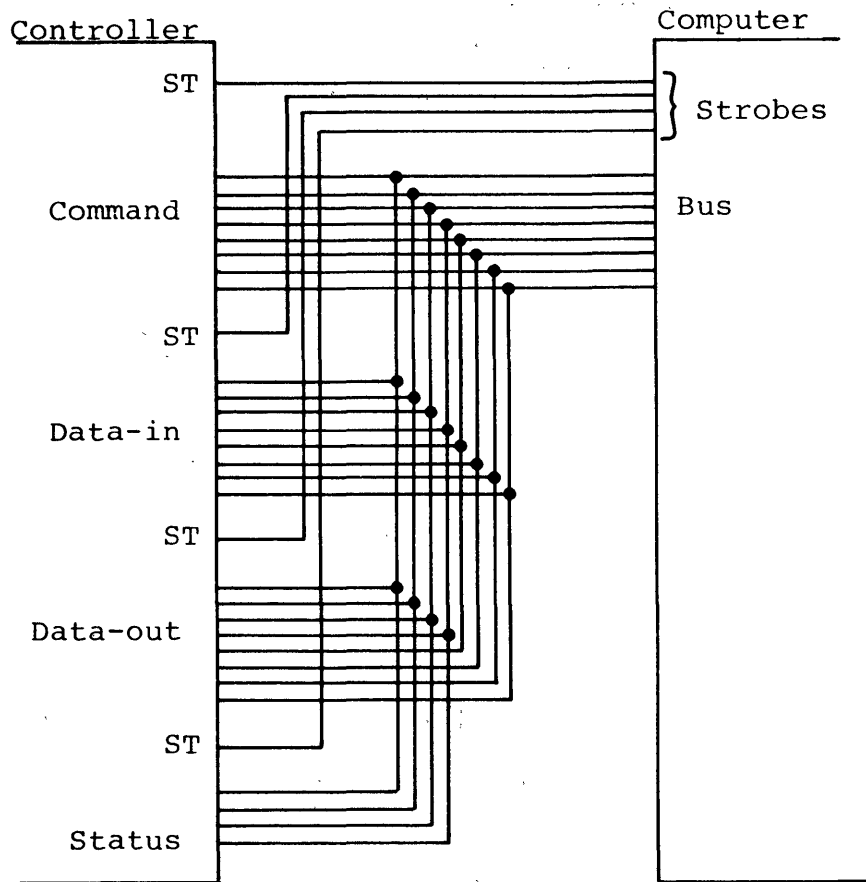


Figure 3.3 Bus Oriented Ports

IV. THEORY OF OPERATION

HEAD ELECTRONICS

The head electronics consists of IC27 and IC28 which drive the head during record and IC13 which amplifies the head signal during read. IC27 and IC28 (75125's) have tri-state outputs which normally are in the high impedance state during a read operation so that they won't influence the low level signal going from the head to the amplifier (IC13). During record, only the sections of IC27 and IC28 associated with the selected drive go into a low impedance state and drive the head in a push-pull manner. R6, R9, R20, and R23 are used to limit the current through the head and should be adjusted for a current of 1.5 times the head saturation current if the standard head is not used. Figure 4.1 shows typical waveforms for the record drivers.

During a read operation, section 1 of IC 13 is used as a pre-amp with balanced inputs and a gain of 3.9. Section 2 is an amplifier with a gain of 22. Section 3 is a low-pass filter and differentiator which produces zero crossings at its output whenever the input signal has a peak. The low-pass filter reduces the differentiator's sensitivity to noise. Section 4 is a Schmitt trigger which detects the zero crossings and produces a TTL compatible signal at its output. Figure 4.2 shows typical waveforms for the read electronics.

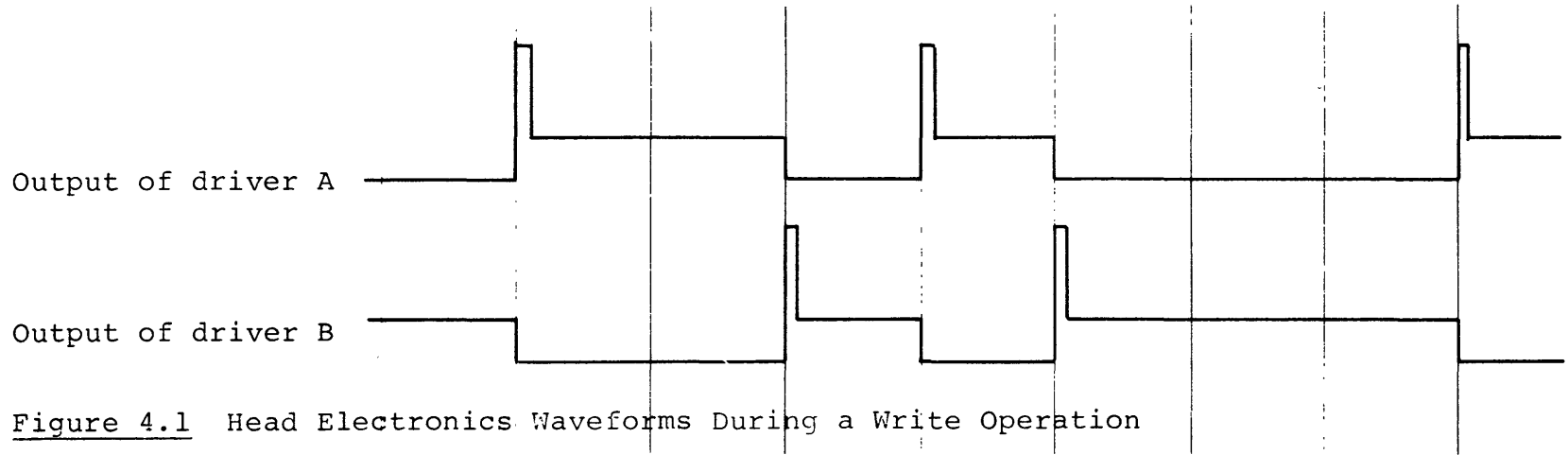
BIT SYNCHRONIZING ELECTRONICS

This section of the controller is used to generate the proper fixed frequency clocks for record and variable frequency clocks synchronized to the data during read. The data is also converted from NRZI encoding to level encoding. This section of the electronics consists of IC9, IC37, IC50, IC41, IC42, IC55, IC10, IC11, T13, and associated logic and components.

IC9 oscillates at 14 times the bit rate (it takes ten of these bits for every eight bit data byte that is recorded) and is adjusted using R28. During read, IC37 and its associated reset circuitry divides the OSC signal by 8 if the data is coming in slow, by 7 if the data is coming in on frequency, and by 6 if the data is coming in fast. The incoming data rate is checked every time there is a data bit of value "1". There is no correction for data bits of value "0". This compensates for small rapid variations in tape speed. Large speed variations generate a DC error voltage with IC10 and IC11 which is fed back to the control input of oscillator IC9. During record, IC37 divides OCS by 7 and T13 turns off the DC feedback loop.

GROUP CODED RECORDING

Since a flux density of 1,600 flux changes per inch was incorporated, a special effort was made to also increase bit density in a packing scheme which maintains self-synchronization. Figure 4.4 illustrates this convention, group-coded recording, in a comparison with some older methods.



Typical
Encoded Data

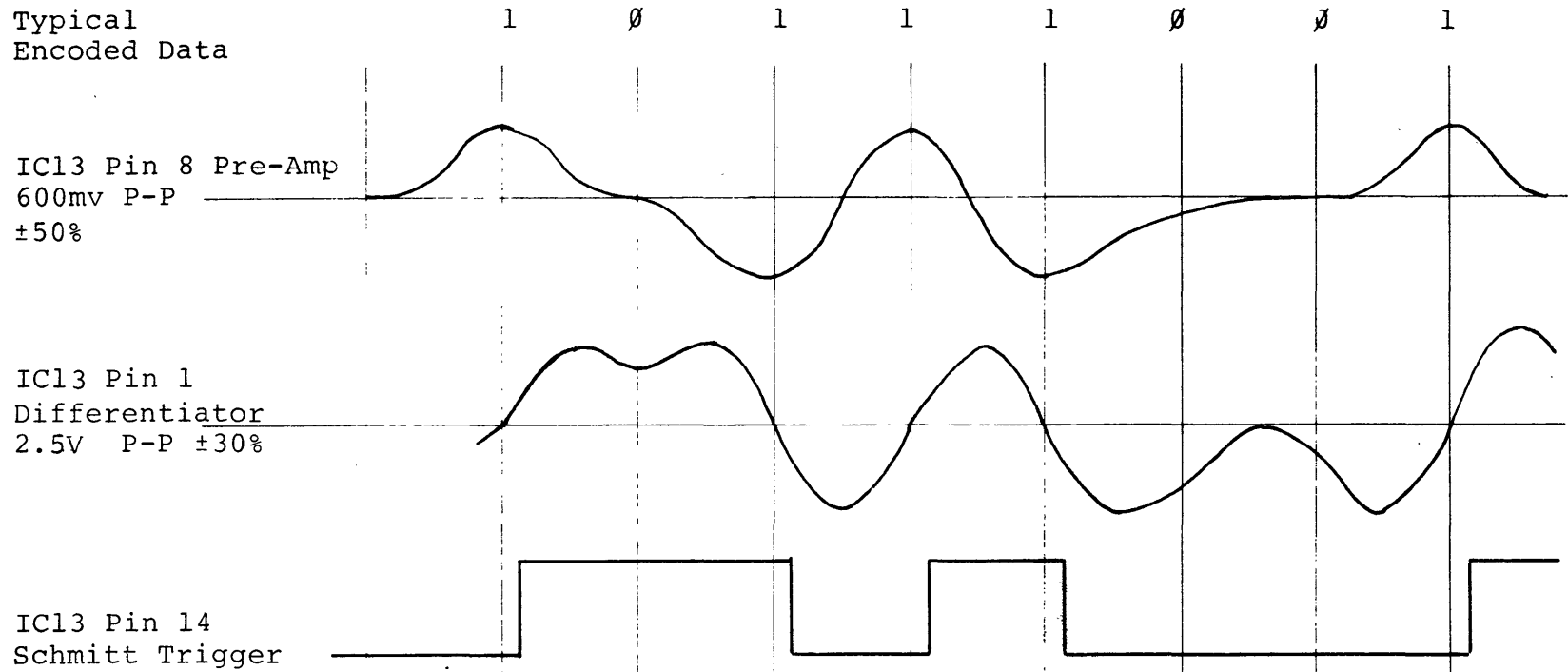
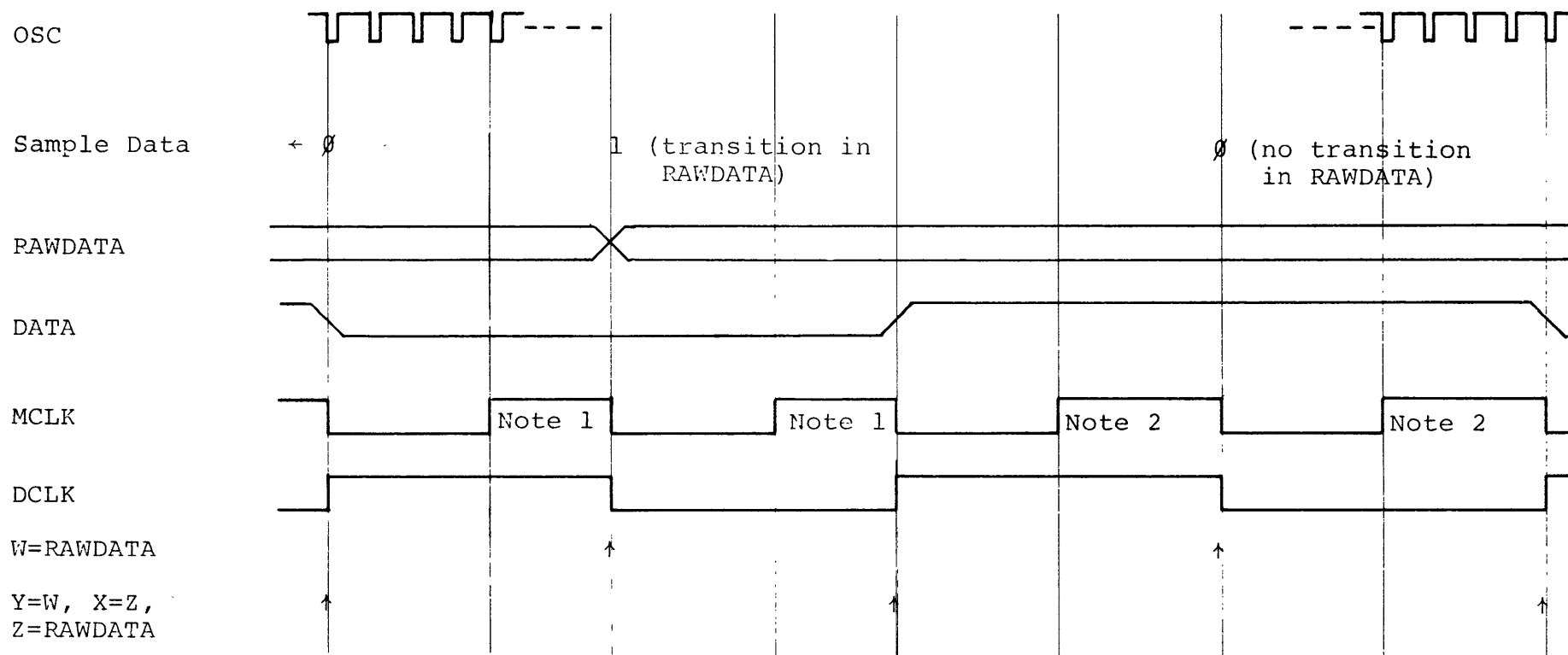


Figure 4.2 Head Electronics Waveforms During a Read Operation



Note 1: This pulse is always 3 OSC cycles if DATA is 0 or RECORDING.

Note 2: This pulse is either 2 or 4 OSC cycles if incoming data is fast or slow respectively and DATA is 1.

Figure 4.3

Bit Synchronizer Timing

NRZI, non-return-to-zero, illustrates a recording efficiency of 1.0, where recording efficiency is defined as the highest ratio of BPI (bits per inch) to FCPI for a given format. There is, at most, only one flux change per bit. Unfortunately, this is not a self-clocking scheme, and is therefore impractical for use on a cassette system which has inherent speed fluctuations.

PE, phase encoding, was designed to overcome such limitations by providing a flux change at the center of each bit period which would synchronize a clocking circuit. The direction of this flux change indicates whether the bit is a 1 or 0. The recording efficiency of this method, however, is only 0.5.

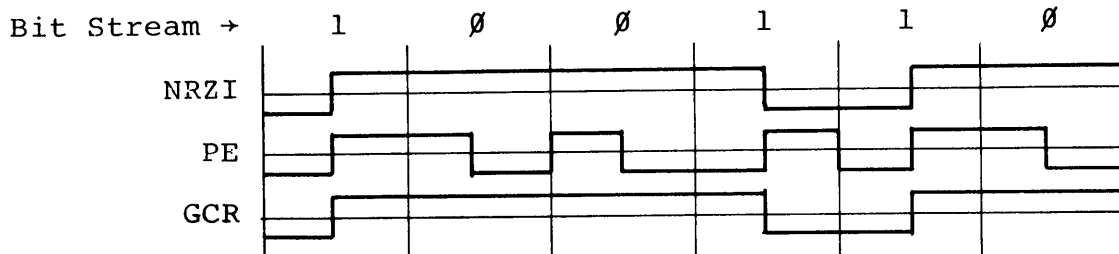


Figure 4.4 Recording Methods

GCR, group-coded recording, at first glance appears very similar to the efficient NRZI method, but with one important difference: No more than two zeros may appear in a row in the bit stream. This guarantees a clock pulse at least once every three bits which provides synchronization. Since a restriction of no more than two zeros in a row cannot be placed on data, a translation scheme is used to encode 4-bit groups into 5-bit groups, and the above restriction is then placed on the 5-bit groups. The translation table is shown in Table 4.5. Since the format is essentially NRZI, we have 4 bits per 5 flux changes, or a recording efficiency of 0.8, which is 60% better than PE.

Table 4.5

4- to 5-Bit Translation Table

<u>4-Bit Data Value</u>	<u>5-Bit Recording Value</u>
0 0 0 0	1 1 0 0 1
0 0 0 1	1 1 0 1 1
0 0 1 0	1 0 0 1 0
0 0 1 1	1 0 0 1 1
0 1 0 0	1 1 1 0 1
0 1 0 1	1 0 1 0 1
0 1 1 0	1 0 1 1 0
0 1 1 1	1 0 1 1 1
1 0 0 0	1 1 0 1 0
1 0 0 1	0 1 0 0 1
1 0 1 0	0 1 0 1 0
1 0 1 1	0 1 0 1 1
1 1 0 0	1 1 1 1 0
1 1 0 1	0 1 1 0 1
1 1 1 0	0 1 1 1 0
1 1 1 1	0 1 1 1 1

RECORDING FORMAT

A synchronous format is automatically added by the electronics to the data being recorded. Of all the 5-bit patterns possible for use in this system, the only pattern not used is lllll. Therefore, this pattern is sent 15 times at the beginning of a data block (75 ones). The purpose of using this pattern is twofold. First, since the start of a block must be found by dropping the head anywhere on the tape, the electronics searches for about 20 ones in a row, and this pattern only occurs at the block start. Second, the ones form a steady clock frequency and allows the self-correcting clocking circuitry to achieve sync in the fastest possible time.

After the ones are recorded, the five bit sequence, 00101, is recorded as a sync character. This particular sequence uniquely defines the absolute start of the block. At that point, the 4 high bits of the first byte are translated to 5 bits and recorded, and then the 4 low bits are translated and recorded. The rest of the bytes are recorded in a similar manner. If a new block is not immediately started, an erase signal will begin after the last byte. Figure 4.6 depicts the format.

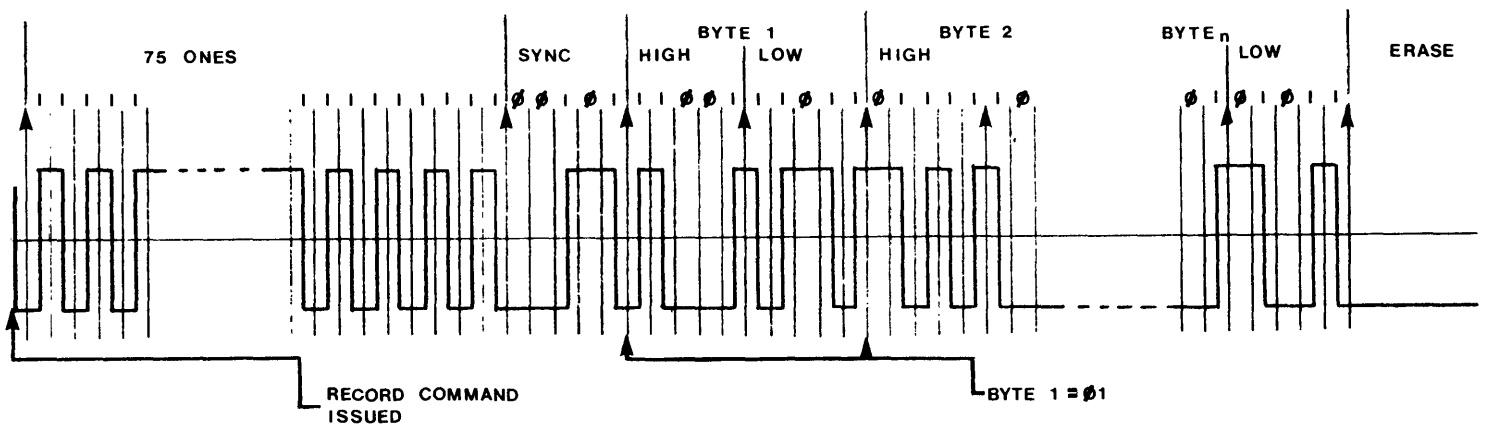


Figure 4.6

Recording Format

DATA FLOW

Record - Data is strobed into IC46 and IC47 with the data input strobe. IC31 and IC32 select the half-byte to be recorded as well as the sync address. IC29 is a ROM which then encodes the 4-bit code into the 5-bit code and sends it to the 5-bit shift register, IC's 30, 5, and 24. The data is then shifted into IC4 which provides the record signal.

Read - Data from the read circuitry is clocked into the 5-bit shift register (IC's 30, 5, and 24). After each half-byte is loaded, data is routed through the selector (IC's 31 and 32) and into the ROM decoder (IC29). Here, the 5-bit code is decoded back into 4 bits and is loaded alternately into IC43 and IC44 to be strobed out.

CONTROL SEQUENCER

The flip-flops whose outputs are RECORD, RUN, B, and A control the sequence of events in the reading and recording processes. Refer to Table 4.7 for the valid sequencer states. The command strobe forces the "SEARCH FOR ONES" state immediately, and system clocks put the sequencer through the appropriate states when the strobe is removed.

For record mode, the sequencer will go to the "GENERATE ONES" state at the next CLOCK1 pulse. The system then waits for IC's 7 and 20 to count out 75 ones and produce the $\overline{\text{ONESDONE}}$ signal. During this time, the ONES signal forces IC29's chip enable to output all ones into the shift register. After the ones are recorded, "SEND SYNC" is entered which produces the $\overline{\text{SYNC-GEN}}$ signal to load a sync pattern into the shift register. Next, "RECORD A" is entered and selects the high bits of the data byte, loading them into the shift register. Finally, "RECORD B" loads and sends the low bits of the data byte. "RECORD A" and "RECORD B" are then alternately repeated until either the next command strobe, a tape stop or jam, or an underrun condition. The latter two events will force the sequencer to the "GAP" or erase state.

Table 4.7

Valid Sequencer States

<u>Function</u>	<u>State</u>			
	<u>RECORD</u>	<u>RUN</u>	<u>B</u>	<u>A</u>
GAP	1	Ø	Ø	1
GENERATE ONES	1	1	Ø	1
RECORD A	1	1	1	1
RECORD B	1	1	1	Ø
SEND SYNC	1	1	Ø	Ø
SEARCH FOR ONES	Ø	Ø	Ø	1
SEARCH FOR SYNC	Ø	1	Ø	1
READ A	Ø	1	1	1
READ B	Ø	1	1	Ø

For read mode, the sequencer remains in the "SEARCH FOR ONES" state until IC's 7 and 20 detect about 20 consecutive ones. If a zero occurs, IC7 is reset and the count begins again. When sufficient ones are found, $\overline{\text{ONEDET}}$ tells the sequencer to go to the "SEARCH FOR SYNC" state. Each read bit is then shifted into IC30 and all five bits in the shift register are selected and routed to the ROM. The SYNC signal occurs when the proper sync bit pattern is found. The "reset to 9" on IC20 is then released and the sequencer is synchronized to the data. Also, the "READ A" state becomes active, and the next five bits of data are shifted in, decoded, and loaded into IC43 as "READ B" is activated. The next five bits are operated on in the same way, except that IC44 is now loaded, and the sequencer goes back to state "READ A."

This sequencer repeats until either a command strobe or an overrun occurs. In the second case, the "SEARCH FOR ONES" state is again forced until the next command strobe.

DATA STATUS LOGIC

READY and OVERRUN/UNDERRUN are controlled by IC21 and only occur at the times the shift register or the data output latches are being loaded. READY is set at the end of state "RECORD B" as the second half-byte of data is loaded into the shift register. It must then be serviced by the time "RECORD A" is entered, since the new first half-byte of data is needed at that point. If READY is not reset at this point (by the input data strobe), OVERRUN/UNDERRUN will latch on.

In read mode, READY is set at the end of state "READ B." It is at this time that the second half-byte of data is loaded into IC44. IF the output data byte is not read before the next half-byte is loaded, the OVERRUN/UNDERRUN flag is latched on.

CLOCKS AND SYSTEM TIMING

There are four major clocking signals derived from a four-phase clock system. MCLK, the master clock, with DCLK, the data clock, generate ECLK, as in Figure 4.8.

IC20 is used to divide DCLK by 5 and get a signal, DIVIDE-BY-5, once every data half-byte. This is combined with other clock phases and sequencer states to obtain the clocks and signals shown in Figure 4.9.

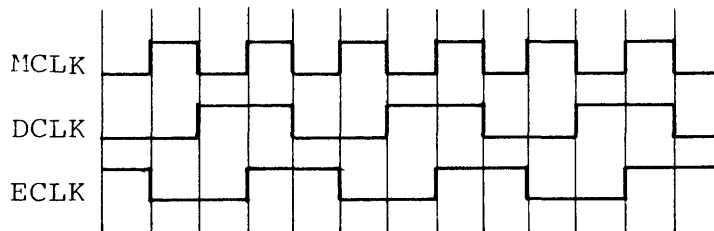


Figure 4.8

4-Phase Clocks

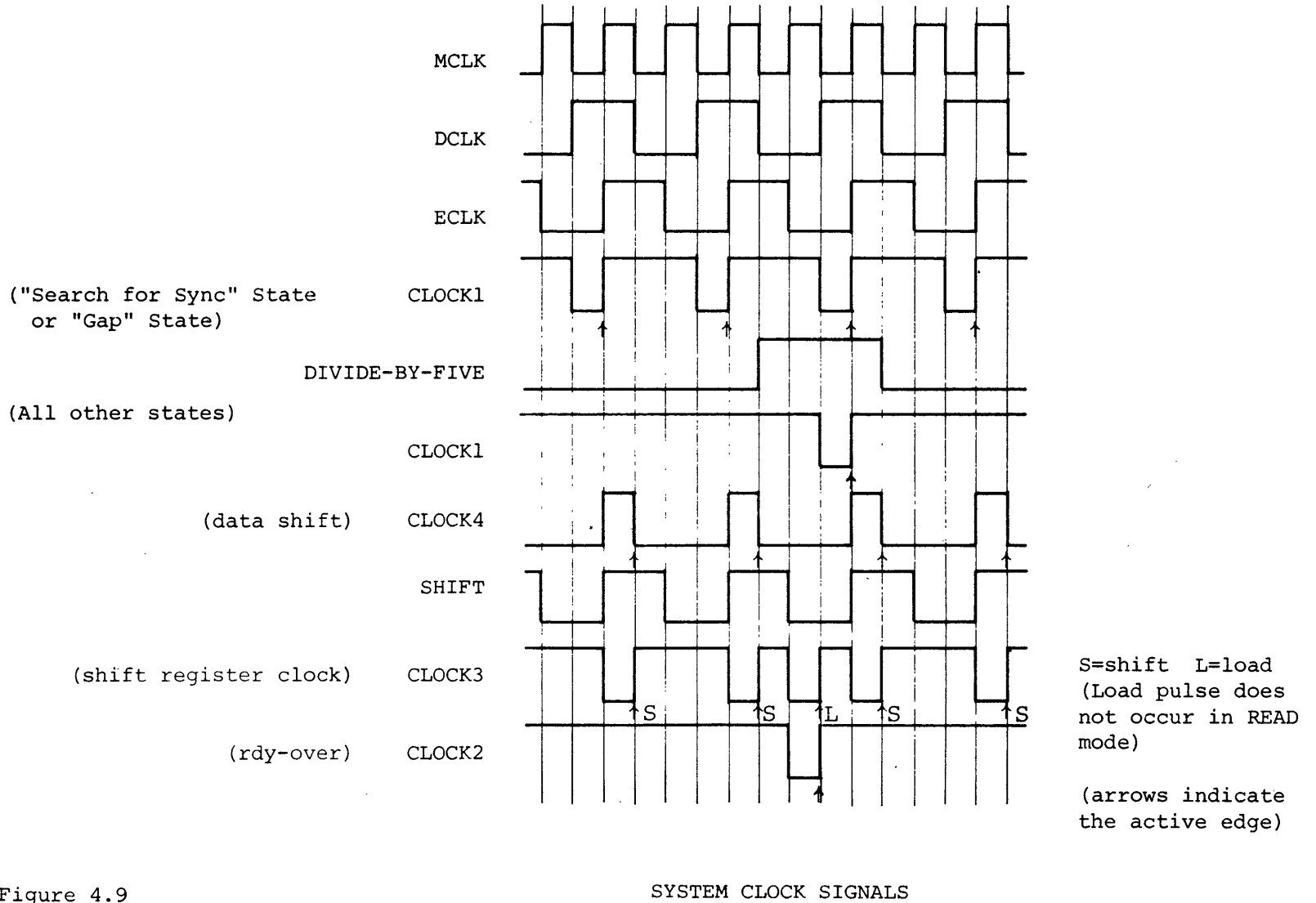


Figure 4.9

SYSTEM CLOCK SIGNALS

MOTOR DRIVE AND SENSE ELECTRONICS

The purpose of this section of the controls is to provide drive to the motors, braking for the motors, deck selection, and sense tape motion for feedback to the motor control electronics.

TAKUPDRV goes to the low state whenever the takeup reel should be driven during read or record. R46 limits the motor torque during this operation. BOTHDRV goes low whenever the motor control electronics senses that the reels should have braking torque applied or that there may be slack tape in the cartridge. R45 limits the torque during this operation. ALCAP is used to turn on the capstan drive motor.

ENGAJDRV goes to the low state whenever the motor control electronics senses that the head and pinch roller should be moved toward or away from the tape. T7, T8, T9, and T10 are used to brake the engage motor whenever it is not being driven. FFDRV and FRDRV are used to drive the tape in the fast forward or fast reverse direction whenever those commands are given.

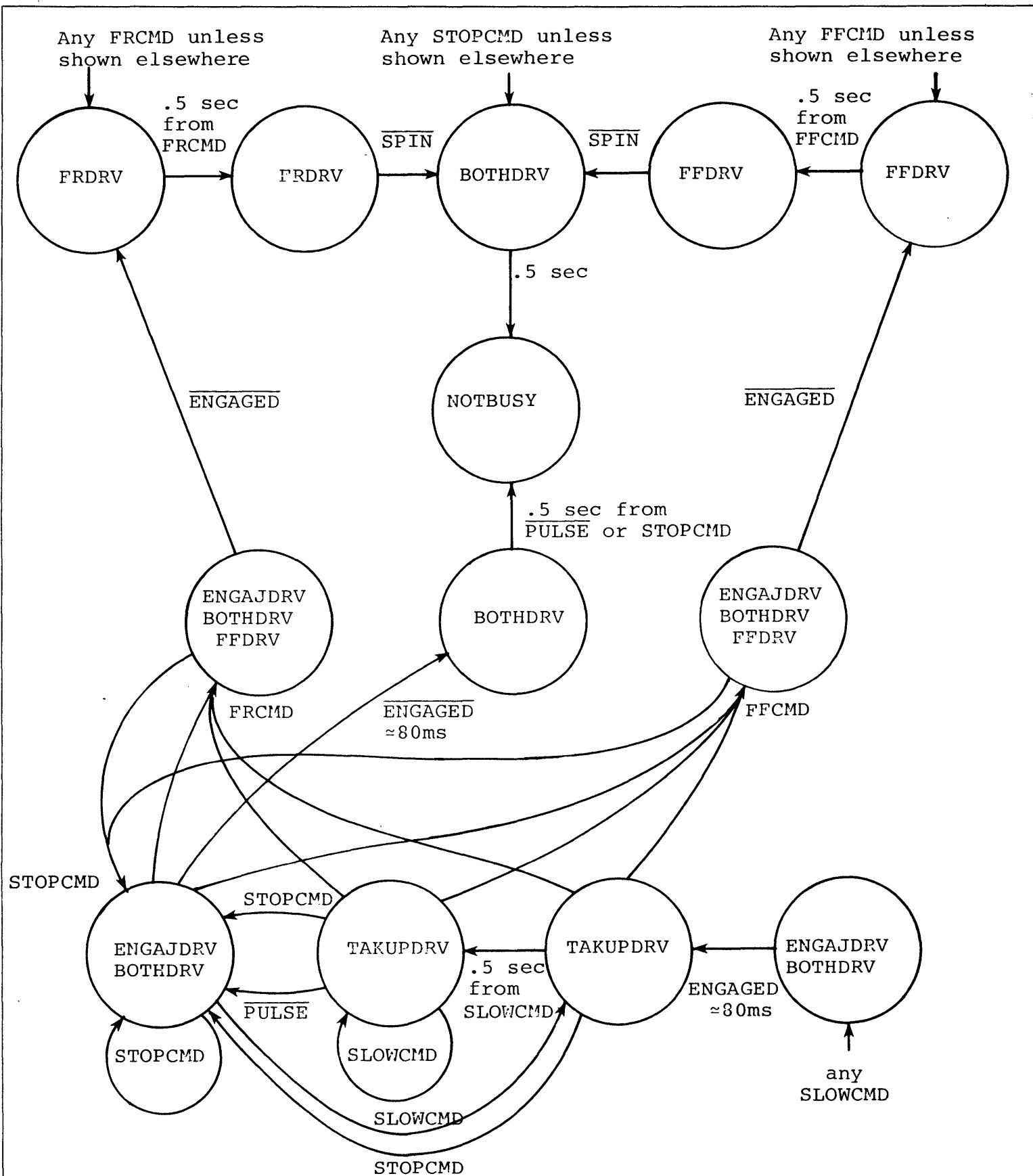
Transistors T2, T3, T4, and T5 in conjunction with steering diodes D1 - D11 and D15 are used to provide drive to the selected deck. Diodes D12, D13 and D14 apply drag to the undriven reel during the fast forward and reverse operations to prevent excessive tape speed and to slow the tape as it nears the end of the reel. Transistors T11 and T12 generate a signal called SPIN which tells the motor control electronics that the undriven reel is turning during the fast forward and reverse operations. The PULSE signal has small negative going pulses on it whenever the takeup reel is turning. This is used to detect tape jams and end of tape during the read, record, or erase operations.

MOTOR CONTROL ELECTRONICS

The motor control electronics senses the status of the tape motion, the position of the headbar, and the commands given by the user and sends control signals to the motor drive circuits. The status bits STOP and NOT BUSY are also generated and sent to the user interface.

The following discussion provides the user with a description of the primary control signals. The user should look at the state diagram given in Figure 4.10 to determine how the deck is actually controlled.

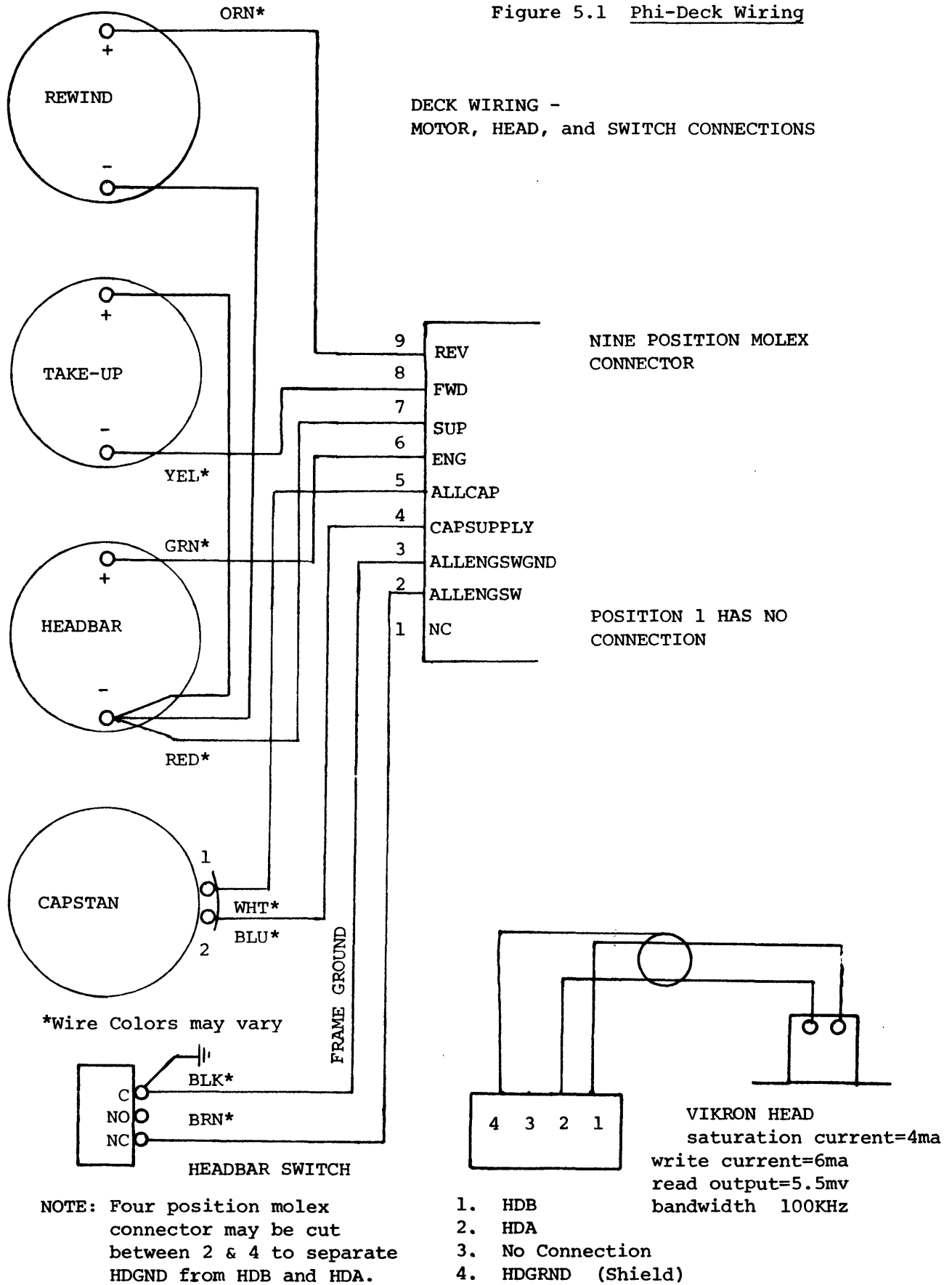
PULSES is generated by a one-shot (IC23) that goes active whenever a command is given and the deck is in the stopped state. PULSES stays active as long as a pulse is received on the PULSE line at least once every half second. If a pulse is not received within the allowed time, PULSES will go to a 1 and cause the deck to go toward the NOT BUSY state. The DELAY signal is also generated by a one-shot (IC23) and is used to inhibit tape motion sensing for 1/2 second after a command is given to allow for the tape to accelerate to the proper speed. This one-shot is also used to time the BOTH signal after a STOP command or tape jam is detected.



Note: Names within circles are motor control signals. Labels on lines indicate commands given by user or events within controller.

Figure 4.10 Motor Control State Diagram

Figure 5.1 Phi-Deck Wiring



QUIT will go to the 1 level if the manual stop button is pressed, if a STOP command is given, if no pulses are detected and there is an active SLOW command, or if SPIN goes low during any FAST command and DELAY is not active. QUIT is equivalent to STOP on the user interface.

V. CONSTRUCTION

Tools:

Fine tipped, low wattage soldering iron, "wire solder" (around 20 gauge resin solder), small diagonal cutters, needle-nose pliers.

Test Equipment:

Voltmeter
500KHz or better oscilloscope
Frequency counter
Microprocessor, Mini, etc.

Estimated Construction Time: 6 - 11 hours

1. Using the component placement chart given in the appendix, insert the 12 16-pin sockets into the PC board. If the sockets have an indicator for pin one, orient it away from the edge connector. Invert the board by placing a book on the sockets to hold them in and carefully solder all pins.
2. Insert and solder the 36 14-pin sockets as described above.
3. Insert and solder the 6 8-pin sockets.
4. The controller and deck need +5 Volts at 1 Amp nominal and +12 Volts at 0.7 Amps peak. Insert IC12, using silicone grease and the heat sink. Solder R57 and R58.
5. Apply power to the board and check voltages. The 9 Volt supply should be between 8.4 and 9.6 Volts. The 5 Volts should be between 4.75 and 5.25.
6. Remove power from the board.
7. Insert and solder the three resistors rated above 1/4 watt (R44, R45, and R46).
8. Insert and solder the data-rate potentiometer (R28). Orient it so that it may be adjusted from the top of the board.
9. Insert and solder the remaining resistors.
10. Insert and solder all polarized capacitors (C2, C13 - C19, C22, C27, C30, C32). C13 and C14 are marked with a + or -. The others have a solid section of color on the positive lead. The board has + notations to aid in orientation.

11. Insert and solder the various remaining capacitors.
12. Insert and solder the four 1N4148 diodes and the 15 1N4001 diodes. All diodes should be oriented so that the bands on the diode are toward the right side of the board. There is also a diode symbol on the board to aid in orientation.
13. Insert and solder T6 - T12 into place. The emitter lead for these transistors is marked with a dot on one of the transistor pads. The appendix contains a pictorial to aid in orienting the various transistors supplied in your kit.
14. Insert and solder the FET (T13). Orient it so that the drain is toward the top of the board (opposite from the connector).
15. Insert and solder T1 - T5. These transistors are placed vertically with the leads inserted fully through the circuit board. Note that the emitter lead is marked with an E on the circuit board.
16. Insert all IC's into their respective sockets, observing correct orientation (pin 1 away from edge connectors).
17. Wire the board into the microprocessor's I/O structure, as described below. Connect the Phi-Deck by slipping the Molex connector supplied with the deck onto pins H - R of the controller's 36-pin socket. Orient the Molex connectors such that the orange wire is on pin R. This puts the deck into position Ø. Remove the protective plastic shield from the digital head on the transport if one has been supplied.
18. If deck 1 will also be used. connect its Molex connector similarly to the connector for deck Ø. Bend the pins out on the 36-pin socket and slip on the connector. Decks 2 and 3 must be rewired at the connector, since several of the necessary signal pins are common to all of the decks.
19. Connect the shielded pair from deck Ø to pins 1 and A. Connect the ground to pin 5 or E. If deck 1 is to be used, connect the shielded pair to pins 2 and B (reverse the connector's orientation) and rewire the ground pin into deck Ø's ground connector. For decks 2 and 3, a different method of connection must be employed, as no more Molex connectors will fit.
20. Proceed with the initial checkout of the board by following the steps under section VII, DEBUG.
21. When the board seems to be working properly, perform the oscillator calibration and read amplifier gain calibration procedures under section VI, CALIBRATION. Calibrate the motor speed only if it is absolutely necessary. The Cassette Storage System is now ready for use.

USING THE CONTROLLER IN A DIGITAL GROUP SYSTEM

The connection diagram in Figure 3.2 of the controller manual is used with the Digital Group Software packages. Most systems will use the wiring chart (Table 6.1).

An optional stop switch may be wired to the controller. A normally open momentary push button which brings the manual stop pin (\bar{B}) to ground will stop all deck movement.

VI. CALIBRATION

Oscillator Calibration - To insure compatibility between decks and tapes among all users of this system, the data rate should be adjusted to meet the standard specifications. Before you proceed with the adjustment of R28, the controller must be placed in the record mode by issuing a record command from the computer. This disables the DC feedback path to pin 5 of IC9. Adjust R28 for a 112 KHz signal at pin 3 of IC9. In record mode, this will produce an 8 KHz signal on DCLK. This bit rate (8,000 bits/sec) will record 1,600 flux changes per inch at a tape speed of five inches per second. The data rate is then 6,400 baud when referenced to the data transfer rate between the computer and the controller.

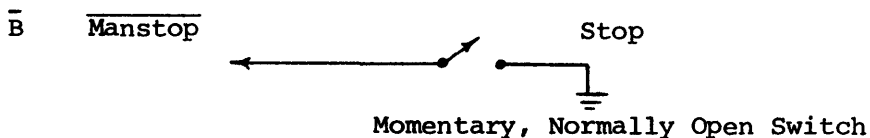
Motor Speed Calibration - The capstan motor on the Phi-Deck is preadjusted to 5 ips at the factory. The following adjustment may be made periodically to keep the deck speed within tolerance. (Note: Side B of your tape has approximately one minute of a 4 KHz test signal recorded on it. This is equivalent to 1,600 FCPI.) Using the 4 KHz test signal recorded on the reverse side of the cassette supplied with your controller, monitor the tape signal in the read mode on IC13, pin 14. With a non-metallic screwdriver or alignment tool, adjust the tape speed through the hole on top of the capstan motor so that the frequency of the tape signal is 4 KHz.

Table 6.1
Wiring Chart

Phi-Deck Board

I/O Board (Ports 0-3)

<u>PIN #</u>	<u>DESCRIPTION</u>	<u>CONNECT TO</u>	<u>PIN #</u>	<u>DESCRIPTION</u>
6	DO7		26	MSB
7	DO6		25	MSB-1
8	DO5 Data		24	MSB-2 Input
9	DO4 Output		23	MSB-3 Port 2
10	DO3 Lines		22	LSB+3
11	DO2		21	LSB+2
12	DO1		20	LSB+1
13	DO \emptyset		19	LSB
14	Data Output Strobe		R	MSB-3, Output Port 1
15	DI7		\bar{D}	MSB
16	DI6		\bar{C}	MSB-1 Output
17	DI5		\bar{B}	MSB-2 Port 2
18	DI4 Data		\bar{A}	MSB-3
19	DI3 Input		Z	LSB+3
20	DI2 Lines		Y	LSB+2
21	DI1		X	LSB+1
22	DI \emptyset		W	LSB
23	Data Input Strobe		U	MSB, Output Port 1
L	* Not Busy		22	LSB+3
M	* Stop	Status	21	LSB+2 Input
N	* Ready	Port	20	LSB+1 Port 2
P	* Overrun/Underrun		19	LSB
R	Status Strobe		S	MSB-2, Output Port 1
S	* Enable/Disable		\bar{D}	MSB
T	* Slow/Fast		\bar{C}	MSB-1
U	* FWD/BKWD	Command	\bar{B}	MSB-2 Output
V	* Stop/Run	Port	\bar{A}	MSB-3 Port 2
W	* RCD/READ		Z	LSB+3
X	* ERASE		Y	LSB+2
Y	* SEL2		X	LSB+1
Z	* SEL1		W	LSB
\bar{A}	Command Strobe		T	MSB-1, Output Port 1



* These pins may actually be wired to the opposite pin on the Phi-Deck Board connector (i.e., pin L to pin 10 on the Phi-Deck Board).

Read Amplifier Gain Calibration - First, record several minutes of test data onto a tape that you will be using. (Once you have decided on a type of tape that gives you good results and that is readily available, you should not change tapes.) Now place the controller in read mode and read your tape. Monitor the signal at IC13, pin 1. If the amplitude is not within the limit shown in Figure 4.2, try different values of R18 until the amplitude is within limits. This adjustment is not critical and your controller will give good results even if your amplitude is not within the limits specified.

VII. DEBUG

Reread the software section to be certain the correct procedures are being executed. Insert controller card (do not connect Phi-Deck yet) and turn power on.

Issue input and output commands to the I/O ports and verify that the strobe signals are present when the command is issued. Also, verify that the data is being latched in the command and data latches correctly (IC33, 46, 47, and 28).

CONNECT THE PHI-DECK AND PROCEED THROUGH THE FOLLOWING SECTIONS.

MOTOR CONTROL ELECTRONICS

Place an old cassette into the deck (if the motor control electronics is not working properly this test may destroy the tape). Issue a fast forward command and check tape movement (these commands are given in the Mechanical Considerations portion of this manual.) Issue a fast reverse command and check tape movement. Remove cassette and issue a stop command. Both reel motors should turn in opposite directions. Reinsert the cassette and issue a record command. The head should engage the tape and the takeup reel should turn. Place your finger on the takeup reel motor pulley. The head should disengage within 1.5 seconds after stopping the motor. If any of the above tests fail, refer to the Theory of Operation for the motor drive and sense electronics and the motor control electronics and proceed to trace the problem.

HEAD SENSE AND BIT SYNCHRONIZING ELECTRONICS

Place controller in record mode and output data bytes to the controller every time READY comes true. You should see waveforms similar to those shown in Figure 4.1 at the outputs of the selected head driver (IC27 or IC28). Waveforms similar to these should also appear on the head of the selected drive.

The read amplifiers may be tested by using the tape you made in the previous paragraph, placing the deck in read mode after rewinding the tape, and looking for the waveforms given in Figure 4.2. If the voltage at IC13, pin 1 is clipping or not within the range shown, refer to Calibration for Adjustment. This adjustment is not critical and is probably not the cause of the controller malfunction.

The bit synchronizing electronics may be checked by verifying the timing diagram shown in Figure 4.3.

READ/WRITE ELECTRONICS

Test all of the clocking signals depicted in Figure 4.9. If a signal is not present or correct, trace back through the logic generating that signal. Make sure about 0.2 Volts of the tape head signal is present on record, and not on read. Check that RECORD reflects the selected state and RDY had a pulsing signal when recording or reading.

The basic clock, IC9, may be removed, and a bounceless switch (Figure 7.1) used to single step the system (14 clocks per data bit). If an oscilloscope is not available, an audio amplifier with the circuit in Figure 7.2 can be used to probe for clocks and data flow. For example, recording or reading in hex "5A" will sound like a 4 KHz square wave on pin 6 of IC5, and (on record) a 2 KHz square wave on pin 3 of IC4. (This signal is not present on erase and read.)

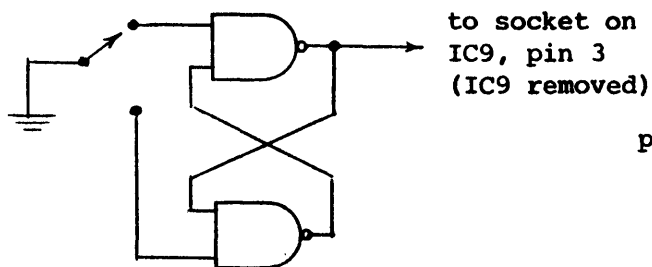


Figure 7.1 Single-step Clock

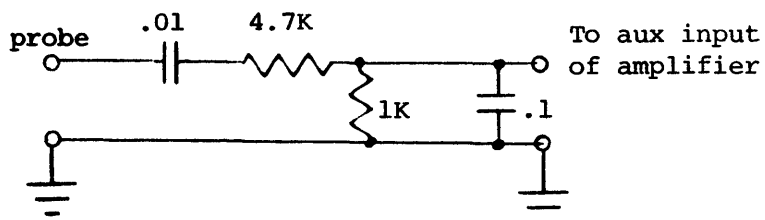


Figure 7.2 Digital to Audio Sensor

VIII. APPENDIX

- A. Parts List
- B. PROM Pattern
- C. Connector Pinout
- D. Component Placement
- E. Schematic
- F. Transistor Orientation
- G. Driver Software Description
- H. Recording Format
- I. Flowcharts
- J. Program Tape and Listings
- K. Phi-Deck Maintenance

A. PARTS LIST

<u>DESCRIPTION</u>	<u>QUANTITY</u>	<u>CIRCUIT REFERENCE</u>
74S00	1	IC49
7400	8	IC1,8,10,14,16,17,25,38,
7402	1	IC15
7404	2	IC34,40
7408	1	IC36
7410	2	IC19,39
7411	1	IC18
7420	2	IC6,22
7451	2	IC2,24
7473	1	IC41
7474	6	IC3,5,21,42,50,55
7475	4	IC33,46,47,48
7486	1	IC26
7490	1	IC20
7493	2	IC7,37
74107	1	IC4
74123	1	IC23
74125	3	IC27,28,45
74153	2	IC31,32
74155	1	IC35
74173,8551	2	IC43,44
74195	1	IC30
74S188,8223,6330-1J	1	IC29
75451	4	IC51,52,53,54
LM324	1	IC13
LM340T-8.0,uA7808	1	IC12
LM358	1	IC11
LM555	1	IC9
2N4403	4	T7,8,9,10
2N5129	1	T12
2N5139	2	T6,11
2N6109	4	T2,3,4,5
2N6410,MJE2050	1	T1
MPF971	1	T13
1.5Ω,1/2W	1	R44
7.5Ω,1W	1	R46
18Ω,2W	1	R45
47Ω	2	R53,57
82Ω	1	R27
220Ω	1	R12
470Ω	1	R48
510Ω	1	R58
680Ω	8	R32,33,34,35,36,37,38,39
1KΩ	7	R6,9,20,23,26,31,55
1.2KΩ	5	R15,16,19,30,42
2.2KΩ	2	R1,29
4.7KΩ	2	R2,49
5KΩPOT	1	R28

<u>DESCRIPTION</u>	<u>QUANTITY</u>	<u>CIRCUIT REFERENCE.</u>
10K Ω	13	R7,8,10,11,14,17,21,22, 24,25,43,47,54
15K Ω	1	R50
22K Ω	2	R40,41
39K Ω	2	R4,5
47K Ω	1	R3
100K Ω	1	R13
150K Ω	2	R51,52
220K Ω	1	R18
1 Meg Ω	1	R56
220pfd mylar	1	C4
.0015mfd mylar	1	C12
.0033mfd mylar	1	C25
.005mfd mylar	1	C3
.01mfd disc	14	C5,6,7,8,9,10,11,20,21, 23,26,28,29,31
.1mfd disc	2	C1,24
1mfd tantalum	10	C2,15,16,17,18,19,22,27, 30,32
100mfd electrolytic	2	C13,14
1N4001	15	D1,2,3,4,5,6,7,8,9,10,11, 12,13,14,15
1N4148	4	D16,17,18,19
TO-220 Heatsink, THM6072B	1	
4-40 Screws	2	
4-40 Nuts	2	
#4 Lockwashers	2	
8-Pin DIP Sockets	6	
14-Pin DIP Sockets	36	
16-Pin DIP Sockets	12	
Dual 22-Pin Edge Connectors	1	
Dual 36-Pin Edge Connectors	1	
PC Board	1	

B. PROM PATTERN

<u>A4</u>	<u>A3</u>	<u>A2</u>	<u>A1</u>	<u>A0</u>	<u>B0</u>	<u>B1</u>	<u>B2</u>	<u>B3</u>	<u>B4</u>	<u>B5</u>	<u>B6</u>	<u>B7</u>
0	0	0	0	0	1	1	0	1	1	1	0	0
0	0	0	0	1	1	1	1	1	0	0	0	0
0	0	0	1	0	1	0	1	0	1	0	0	0
0	0	0	1	1	1	0	1	1	0	0	1	0
0	0	1	0	0	1	1	0	1	1	1	0	0
0	0	1	0	1	1	0	0	1	0	0	0	1
0	0	1	1	0	1	0	1	0	1	0	0	0
0	0	1	1	1	1	0	1	1	1	0	1	0
0	1	0	0	0	1	1	1	0	1	1	1	0
0	1	0	0	1	0	1	0	1	1	0	1	0
0	1	0	1	0	0	1	1	0	1	1	0	0
0	1	0	1	1	0	1	1	1	1	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1	0
0	1	1	0	1	0	1	0	1	1	0	1	0
0	1	1	1	0	0	1	1	0	1	1	0	0
0	1	1	1	1	0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	0	0	0	1	1	0
1	0	0	0	1	0	0	0	0	0	1	0	0
1	0	0	1	0	0	0	0	0	0	1	0	0
1	0	0	1	1	0	0	0	0	0	1	1	0
1	0	1	0	0	0	0	0	0	0	1	1	0
1	0	1	0	1	0	0	0	0	0	0	1	0
1	0	1	1	0	0	0	0	0	0	1	0	0
1	0	1	1	1	0	0	0	0	0	1	1	0
1	1	0	0	0	0	0	0	0	0	0	1	0
1	1	0	0	1	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0	0
1	1	0	1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1	0	0
1	1	1	0	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	1	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1	0
1	1	1	1	1	0	0	0	1	0	0	1	0

C. CONNECTOR PINOUT

Top of Card - Component Side

<u>Pin No.</u>	<u>Description</u>
1	HDA \emptyset
2	HDA1
3	HDA2
4	HDA3
5	HDGND
6	DO7
7	DO6
8	DO5 Data
9	DO4 Output
10	DO3 Lines
11	DO2
12	DO1
13	DO \emptyset
14	Data Output Strobe
15	DI7
16	DI6
17	DI5
18	DI4 Data
19	DI3 Input
20	DI2 Lines
21	DI1
22	DI \emptyset
23	Data Input Strobe
24	+9V Out
25	ENG3
26	SUP3
27	FWD3
28	REV3
29	ALLENGSW
30	ALLENGSWGND
31	CAPSUPPLY
32	ALCAP
33	ENGL
34	SUP1
35	FWD1
36	REV1

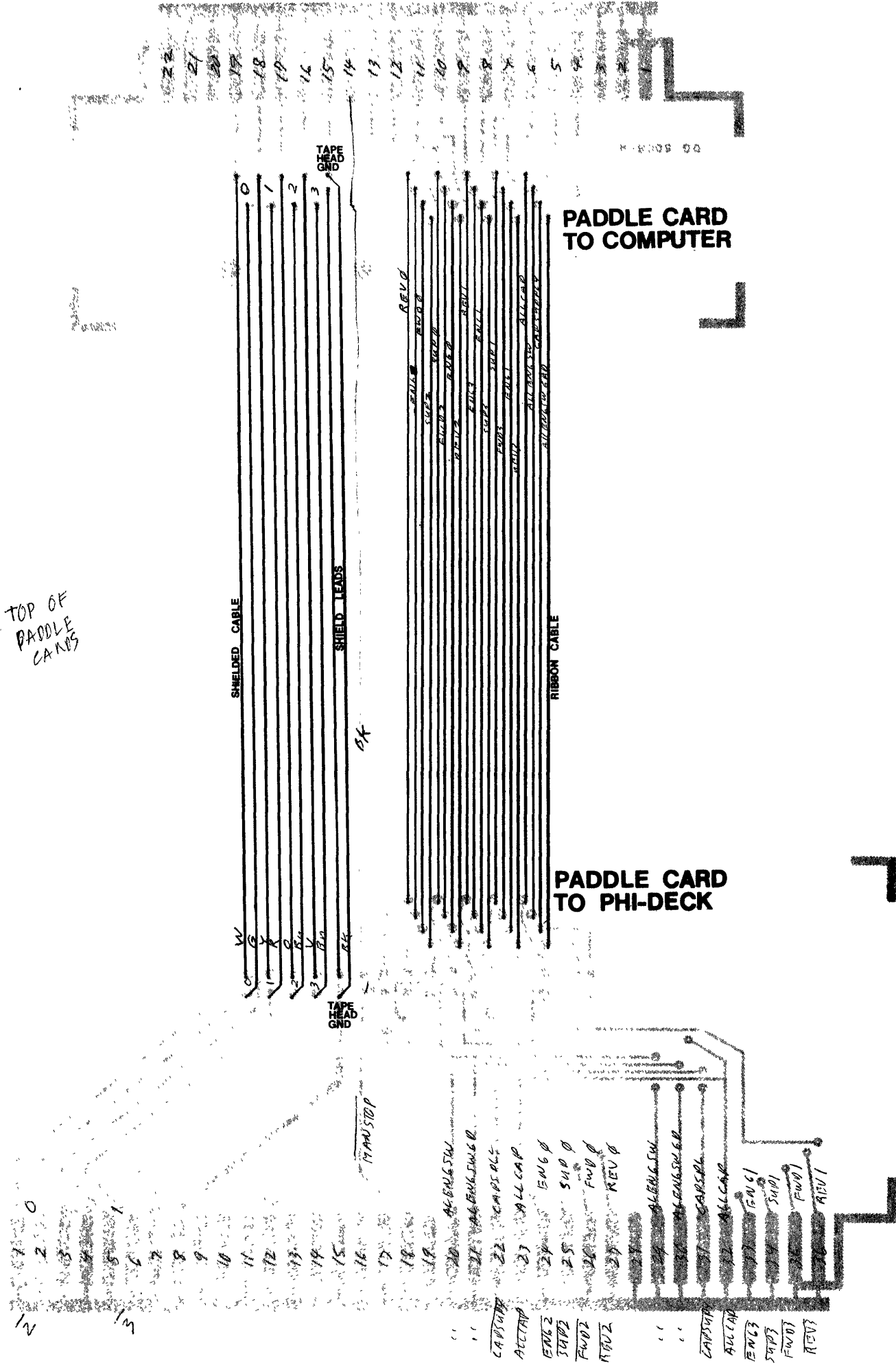
Bottom of Card - Circuit Side

<u>Pin No.</u>	<u>Description</u>
A	HDB \emptyset
B	HDB1
C	HDB2
D	HDB3
E	HDGND
F	DATA READY IRQ
H	n/c
J	n/c
K	n/c
L	Not Busy
M	Stop Status
N	Ready Port
P	Overrun/underrun
R	Status Strobe
S	Enable/Disable
T	Slow/Fast
U	FWD/BKWD Command
V	Stop/Run Port
W	RCD/READ
X	ERASE
Y	SEL 2
Z	SEL 1
\bar{A}	Command Strobe
\bar{B}	\bar{M} anstop
\bar{C}	ENG2
\bar{D}	SUP2
\bar{E}	FWD2
\bar{F}	REV2
\bar{H}	ALLENGSW
\bar{J}	ALLENGSWGND
\bar{K}	CAPSUPPLY
\bar{L}	ALCAP
\bar{M}	ENG \emptyset
\bar{N}	SUP \emptyset
\bar{P}	FWD \emptyset
\bar{R}	REV \emptyset

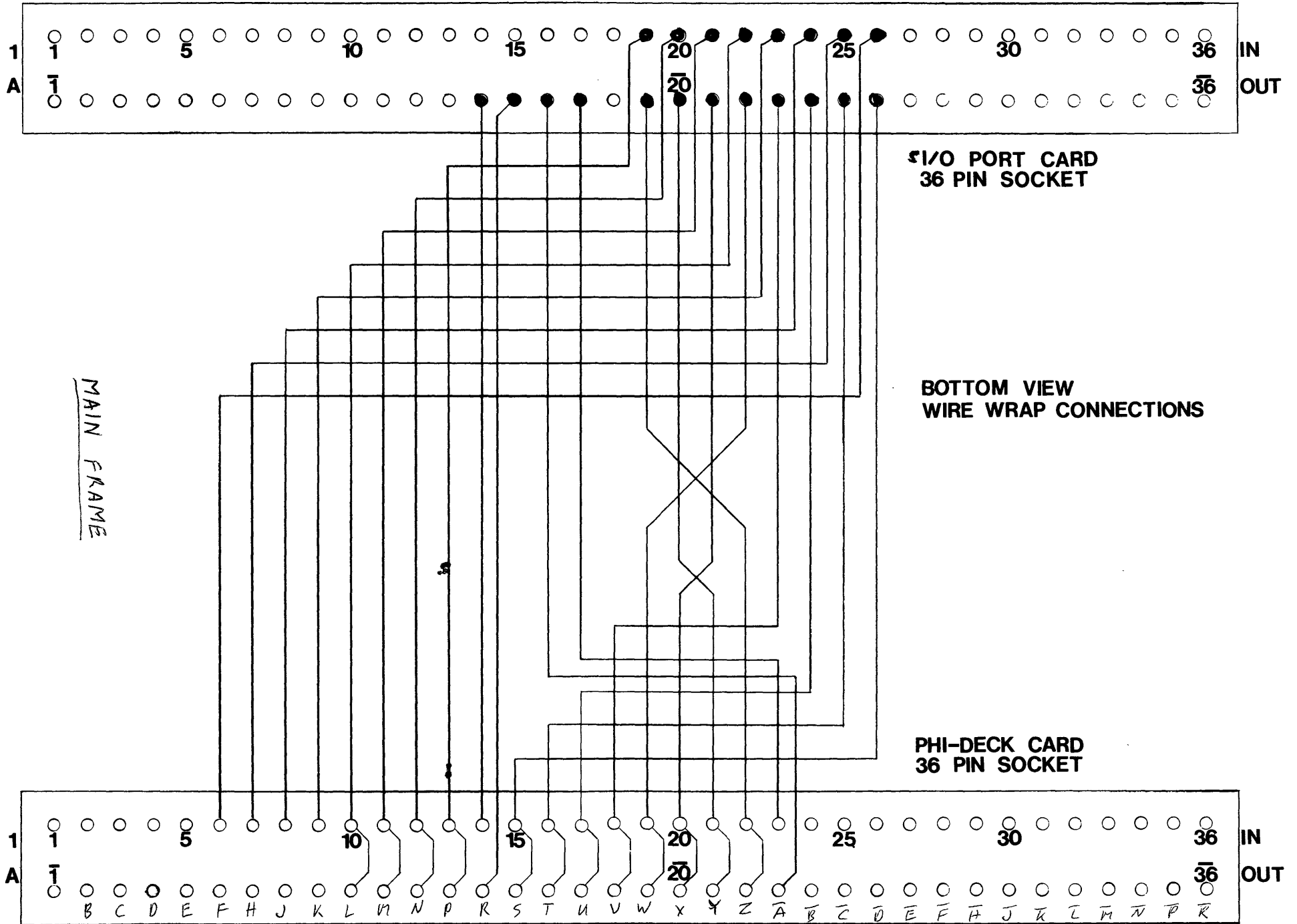
Note: n/c = no connection
 Pin 1 on 22-pin connector = +5V
 Pin 2 on 22-pin connector = GND
 Pin 22 on 22-pin connector = +12V

DETAIL 3

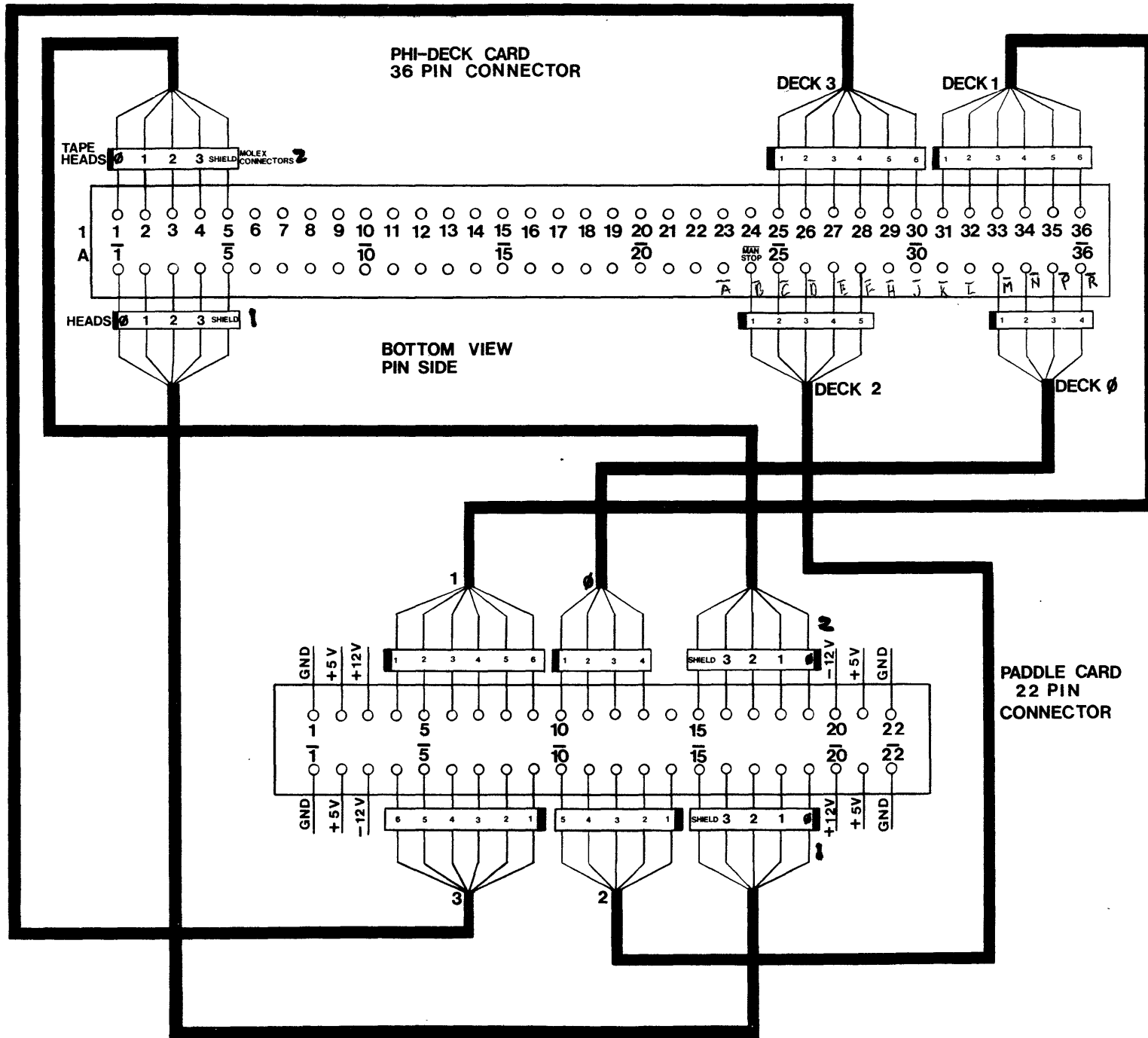
TOP OF
PADDLE
CAMPS



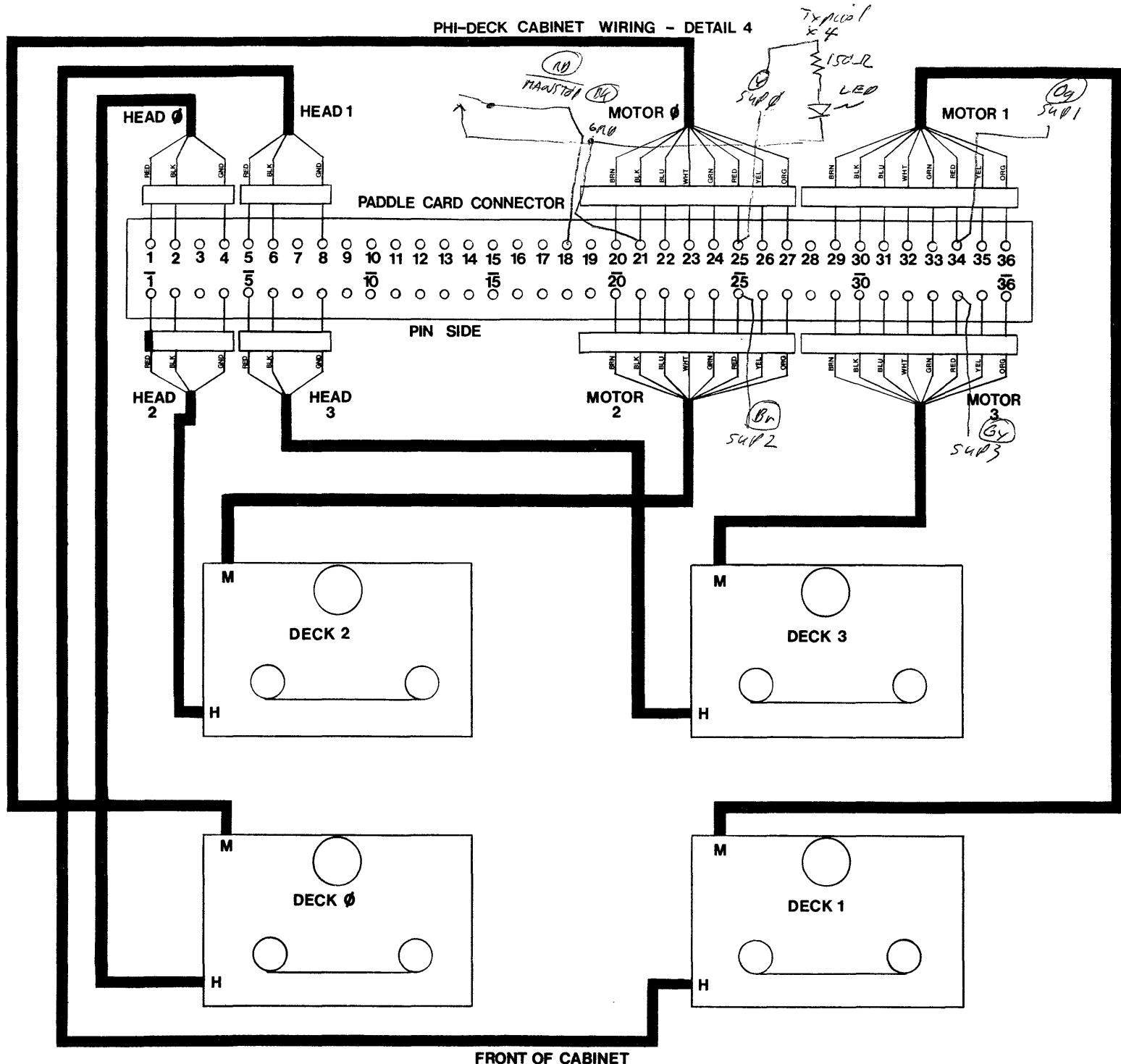
CONNECTIONS BETWEEN CARDS - DETAIL 1



PHI-DECK CARD CONNECTIONS TO
PADDLE CARD BACKPLANE - DETAIL 2

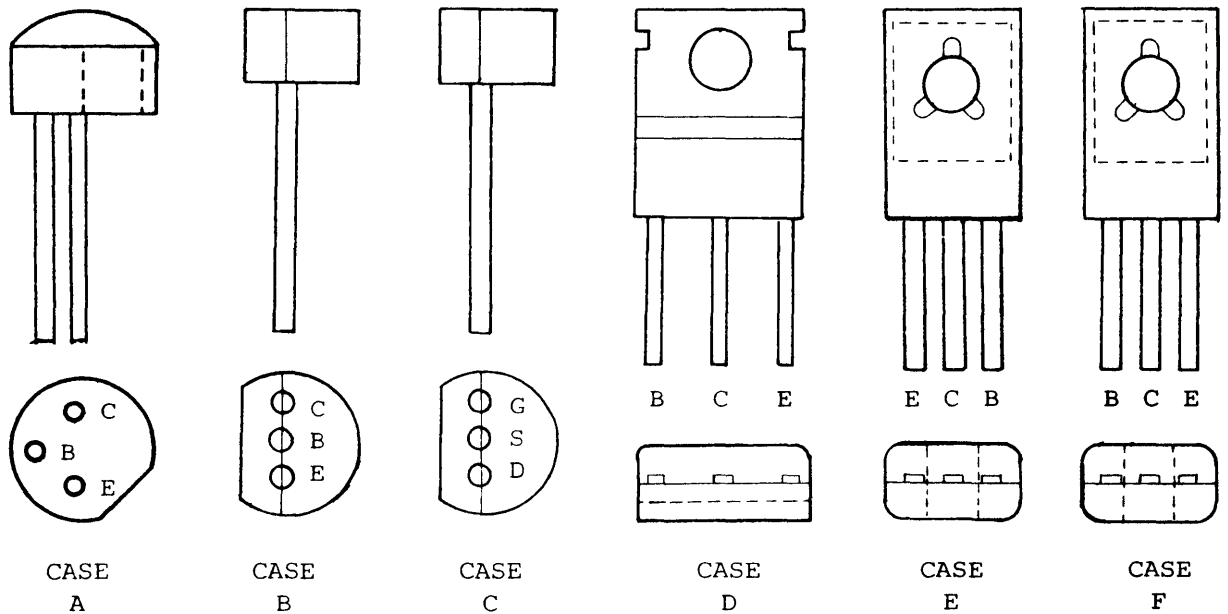


PHI-DECK CABINET WIRING - DETAIL 4



FRONT OF CABINET

F. TRANSISTOR ORIENTATION



Transistor

2N6109
 2N5139
 2N5129
 2N4403
 2N6410
 MJE2050
 MPF971

Case

D
 A or B
 A or B
 B
 F
 E
 C

G. DRIVER SOFTWARE DESCRIPTION

The software supplied with the Digital Group Cassette Storage System contains deck control subroutines to allow the user to concentrate on applications. The READ and RECORD routines provide all error recovery during read, and data verification during record.

The software package consists of several major routines to aid the user in controlling the decks. These are the RECORD, CMDOUT, READ, and REWIND routines. There are numerous minor subroutines the user may invoke if he feels the need to control the deck on a more basic level.

The sample 8080 program given below is a simple example of how to use the major routines. The sample program will read the tape on deck 0 and write the data on deck 1, one block at a time. This program will halt if an unrecoverable error occurs. The major routines are described in more detail following the example. (Note: The sample Z80 program may be found under Program Listings.)

* SAMPLE PROGRAM TO COPY A TAPE
* ON DECK 0 TO A TAPE ON DECK 1
* ONE BLOCK AT A TIME

<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
START	MVI	A,0	SET DECK 0
	STA	DECK	
	CALL	REWIND	REWIND DECK 0
	MVI	A,1	SET DECK 1
	STA	DECK	
	CALL	REWIND	REWIND DECK 1
	SUB	A	CLEAR REGISTER A
	STA	TEMPID	INITIALIZE ID
REDBLK	IN	TAPEIN	WAIT FOR NOT BUSY
	ANI	08H	BECAUSE THE DECK
	JZ	REDBLK	NUMBER IS CHANGING
	MVI	A,0	SET DECK 0
	STA	DECK	
	LXI	H, BUFFER	SET UP POINTER
	SHLD	POINTR	
	LDA	TEMPID	SET UP ID
	STA	IDR	
	MVI	E,0	SET READ MODE
	CALL	READ	READ BLOCK
	PUSH	PSW	SAVE REGISTER A
	MVI	C, F0H	STOP DECK
	CALL	CMDOUT	
	POP	PSW	RESTORE REGISTER A
	CPI	0	ERROR?
	JZ	WRTBLK	NO
	CPI	2	BLOCK FOUND?

<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
	RZ		NO, FINISHED
	HLT		HALT BECAUSE ERROR
WRTBLK	IN	TAPEIN	WAIT FOR NOT BUSY
	ANI	Ø8H	BECAUSE THE DECK
	JZ	WRTBLK	NUMBER IS CHANGING
	MVI	A,1	SET DECK 1
	STA	DECK	
	LXI	H,BUFFER	SET UP POINTER
	SHLD	POINTW	
	LDA	TEMPID	SET UP ID
	STA	IDW	
	INR	A	INCREMENT ID
	STA	TEMPID	
	MOV	A,B	SET UP COUNT
	CPI	Ø	256?
	JZ	X256	YES
	MOV	L,B	
	MVI	H,Ø	
	JMP	CALRCD	
X256	MVI	H,1	
	MVI	L,Ø	
CALRCD	CALL	RECORD	RECORD BLOCK
	CPI	Ø	ERROR?
	JZ	REDBLK	NO, COPY NEXT BLOCK
	HLT		HALT BECAUSE ERROR
TEMPID	DS	1	
BUFFER	DS	256	
	END		

The REWIND routine will stop the operating deck, select the specified deck, and rewind it. This routine returns to the calling routine after the selected deck has been rewound and readied for another command. Memory location "DECK" must contain the selected deck number (in binary) before the routine is called.

The RECORD routine will record data in the standard block format and then check the recorded data to verify that it was recorded without error. If an error is detected, that portion of the tape is erased and all the remaining data is re-recorded. This process is repeated until all data has been recorded successfully, or an unrecoverable error is detected.

As the user records data he must record blocks in sequence starting with IDW = Ø,1,2, etc. Numbers may not be skipped! After a series of blocks have been recorded, the user may re-record a block, but all old blocks following the new blocks may be lost. Although not absolutely necessary, it is recommended that tapes be erased with a bulk eraser or using the Phi-Deck in erase mode to obtain maximum performance and prevent the controller software from becoming confused with the old data.

In order to use this routine properly, the input variables must be set up properly:

1. The deck number must be placed in memory location DECK.
2. The low order byte of the block ID must be placed in memory location IDW, and the high order byte must be placed in IDW+1.
3. The low order byte of the address of the first byte to be recorded is placed in memory location POINTW, and the high order byte is placed in POINTW+1.
4. The number of bytes to be recorded is placed in register pair H and L. A count of zero will cause the record routine to simply return without recording any data.

When the record routine returns control to the calling routine, the registers and memory are modified as follows:

1. All Registers are altered.
2. IDW returns the ID of the last block recorded plus one.
3. POINTW points one location greater than the last byte recorded.
4. The error code is returned in the A register and should be checked after every call to the RECORD routine. The error codes are:
 - Ø - Record completed with no errors
 - 1 - CRC error in block ID-1
 - 2 - Block ID-1 not found
 - 3 - End of tape or jam

The READ routine will read one block and return to the calling routine. The deck is left running so the user must either read another block or issue a stop command to the deck directly (see the CMDOUT routine).

To use this routine the following variables must be set up properly:

1. The deck number is placed in memory location DECK.
2. Memory location IDR contains the low order byte of the ID of the block to be read. IDR+1 contains the high order byte.
3. Memory location POINTR contains the low order byte of the address of the data that is to be deposited. POINTR+1 contains the high order byte.
4. Register E contains the mode. Ø indicates that the data block is to be read into memory starting at the location specified by POINTR. 1 indicates that the data block is to be checked for errors only (in this mode POINTR is not used).
5. RETRYS (Register D) should be initialized only if the ALTRD or ALTRD2 entry points are used. It is automatically initialized to 10 if the READ entry point is used. The user should normally use the READ entry point.

When the read routine returns control to the calling routine, the registers and memory are modified as follows:

1. Registers A,B,C,D,H, and L are modified.

2. COUNT (Register B) contains the number of bytes contained in the block:
 - ∅ = 256 bytes
 - 1 = 1 byte
 - 2 = 2 bytes
 - 255 = 255 bytes
3. ERROR (Register A) contains the error code after a read operation has been completed. The error codes are:
 - ∅ - No errors
 - 1 - Unrecoverable data error
 - 2 - Unable to find block specified by ID
 - 3 - End of tape or jam

The CMDOUT routine is used to issue commands to the transport. Memory location DECK must contain the number of the deck that is referenced by the command. Register C must contain the command to be issued to the deck. The valid commands are:

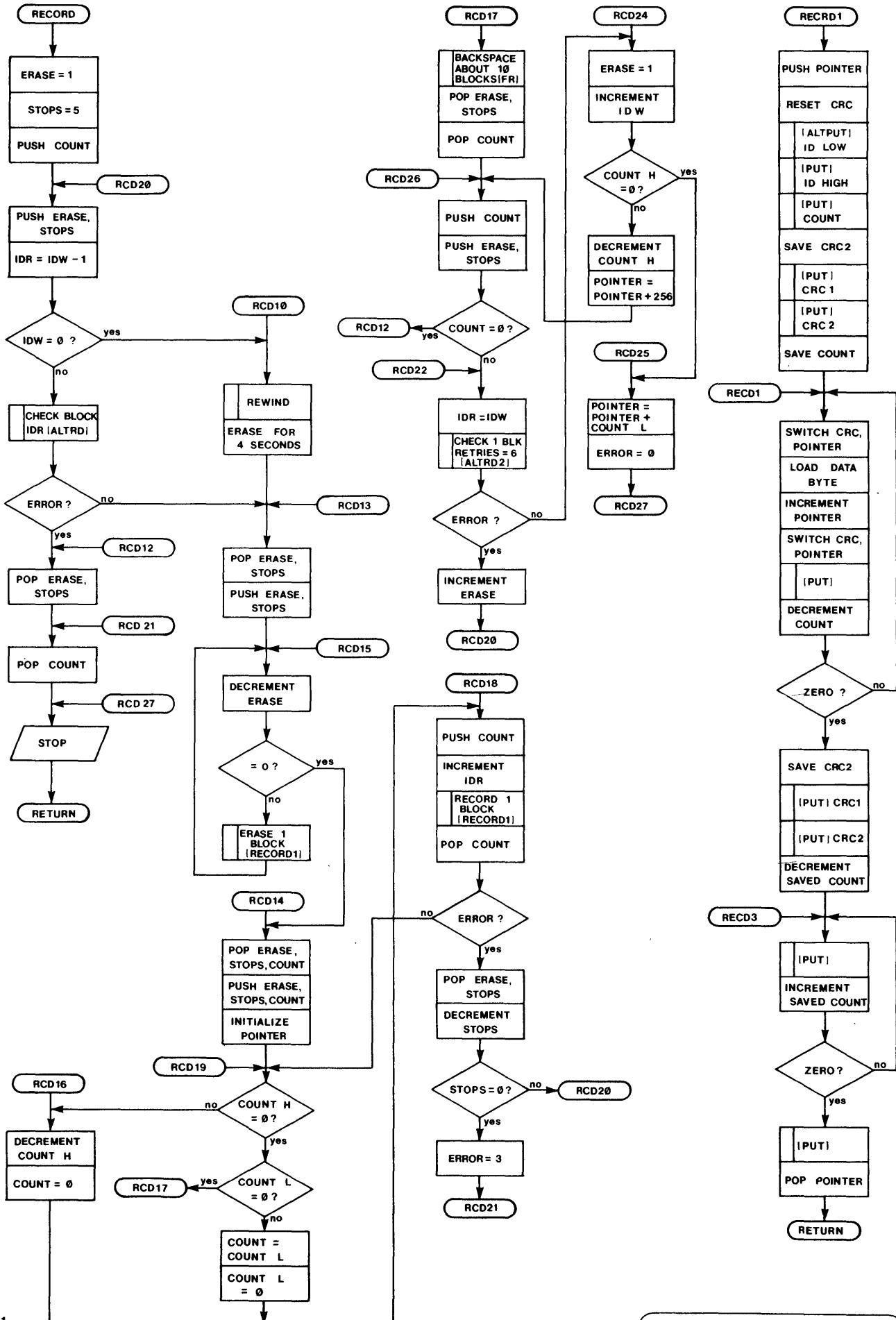
<u>COMMAND</u>	<u>VALUE IN REGISTER C</u>	
STOP	1 1 1 1	0 0 0 0
FAST FORWARD	1 0 1 0	0 0 0 0
FAST REVERSE	1 0 0 0	0 0 0 0
READ	1 1 1 0	0 0 0 0
RECORD	1 1 1 0	1 0 0 0
ERASE	1 1 1 0	1 1 0 0
STANDBY	0 1 1 1	0 0 0 0

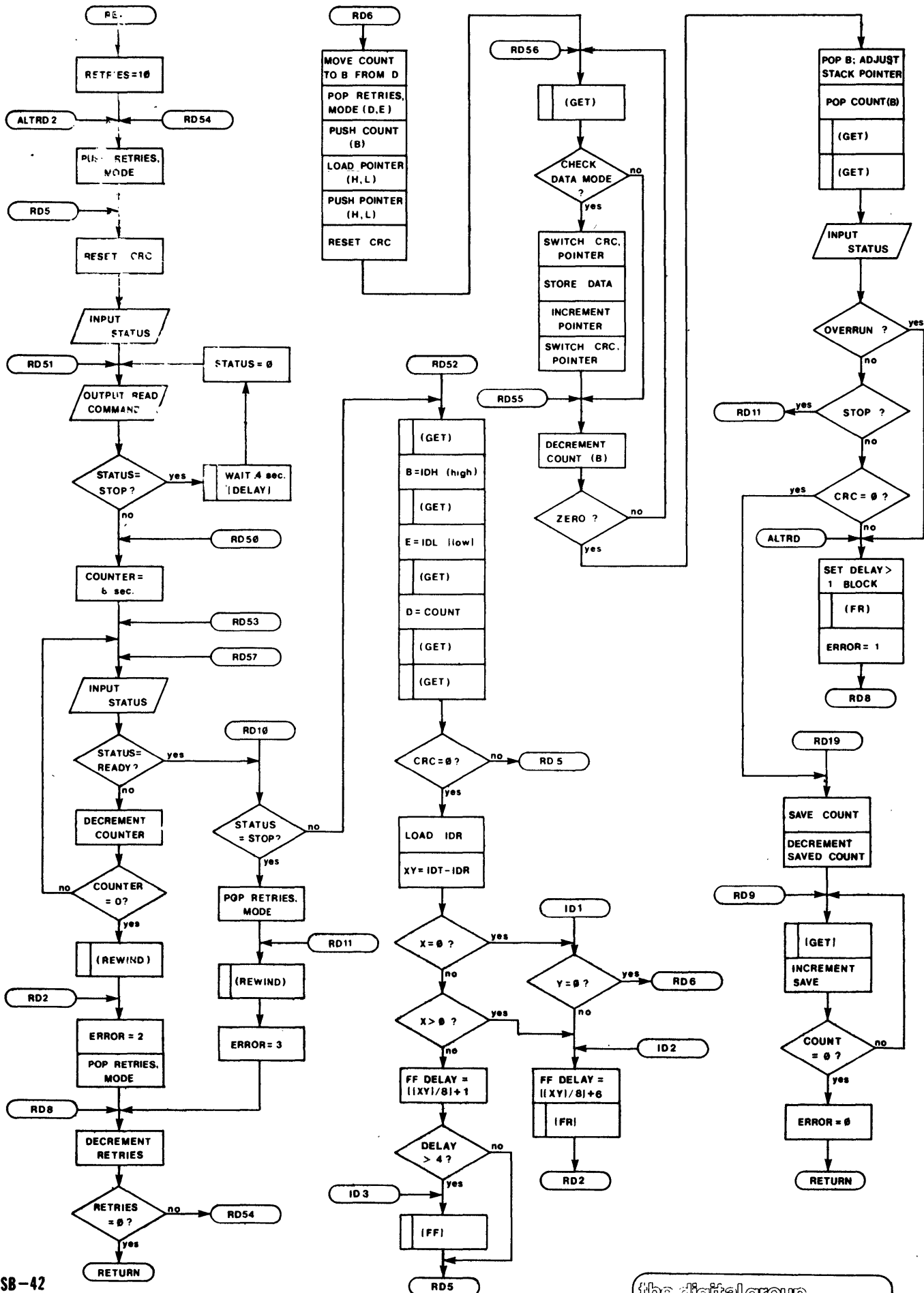
H. RECORDING FORMAT

This appendix shows the block format as it is recorded on the tape by the driver software and controller. Each byte recorded on the tape consists of 10 bits or flux changes (see hardware description).

<u>DESCRIPTION</u>	<u>BYTES RECORDED</u>
75 one bits	7.5
SYNC character	.5
ID high	1.
ID low	1.
COUNT	1.
CRC 1	1.
CRC 2	1.
DATA	1. to 256
CRC 1	1.
CRC 2	1.
TOTALS*	<u>16 to 271</u>

*The record routine will erase to an equivalent of 271 bytes for short blocks so that all blocks will be the same size.





J. PROGRAM TAPE AND LISTINGS

```
*****  
*  
* The tape supplied with the program listing is an *  
* AUDIO CASSETTE recorded at 1100 Baud in Suding *  
* format. This WILL NOT load from the PHI-DECK. *  
*****
```

The program tape contains four programs in the following order:

1. Phi-Deck Demo for Z-80
2. Z-80 Ops System
3. Phi-Deck Demo for 8080
4. 8080 Ops System

Each program includes the PHI-DECK driver routines in the program listing in locations 0900H thru 0B9DH (011000 thru 013235).

Z-8Ø PHI-DECK DEMO SOFTWARE

1. Programs are loaded via audio cassette.
2. At completion of a successful load a listing of Phi-Deck commands will be displayed.
3. In addition to the displayed options, there are three possible options - "R", "S", and "P".
4. "R" will return control to the Z-8Ø Ops System which includes:
 - 1 Read - Read an audio cassette
 - 2 Write - Write an audio cassette
 - 3 Octal Dump - Storage Dump in octal
 - 4 Octal Program - User programming in octal
 - 5 Hex Dump - Storage Dump in hex
 - 6 Hex Program - User programming in hex
 - 7 Phi-Deck Ops
5. "S" will display memory in either hex or octal depending upon last option (hex or octal) chosen by the user.
6. "P" will allow user to program as in Z-8Ø Ops System in either hex or octal depending upon last method chosen in Z-8Ø options 3 thru 6.
7. Reset will return control to Phi-Deck ops.
8. "P", "R", and "S" will operate when in Storage Dump, Program, or Phi-Deck Ops.
9. Phi-Deck option "#" allows the user to select any of 4 decks (Ø-3) by pressing shift # then desired deck number. To return to Phi-Deck Ops press Y. The selected deck number will be displayed in the options listing upon return.
10. Phi-Deck option "Ø" will copy a tape from deck Ø to deck 1. This is not intended as an efficient method of duplicating tapes, only as a demonstration of Phi-Deck routines.
11. Page Ø15 is being used as a 256 byte buffer in the Copy Tape option.
12. Phi-Deck option "1" will erase a tape on the selected deck.
13. Phi-Deck option "2" will fast reverse the selected deck.
14. Phi-Deck option "3" will fast forward the selected deck.
15. Phi-Deck option "4" will place all decks in standby. The capstan motors will be turned off.
16. Phi-Deck option "5" will stop the selected deck.
17. Phi-Deck option "6" will issue a read command to the selected deck. This will not read data from a tape.
18. Phi-Deck option "7" will issue a record command to the selected deck. This will not record data on a tape.
19. Phi-Deck option "8" will record 256 byte blocks of data in a fixed pattern.
20. Phi-Deck option "9" will read 256 byte blocks of data from a tape in a fixed pattern. An "e" will be displayed on the monitor for blocks in error and a "g" for good blocks.

CHANGES TO Z-80 OPERATING SYSTEM
FOR PHI-DECK DEMO

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
054E	00				Address for key 7
054F	07				
05F0	13				Spaces
05F1	B7				7
05F2	A0				
05F3	D0				P
05F4	C8				H
05F5	C9				I
05F6	A0				
05F7	C4				D
05F8	C5				E
05F9	C3				C
05FA	CB				K
05FB	A0				
05FC	CF				O
05FD	D0				P
05FE	D3				S
05FF	00				Return
0103	00		RST	8	
0104	07				
0401	03				
0402	05				
04D6	03				
04D7	05				
0500	C3				
0501	00				
0502	07				

Z-80 PHI-DECK DEMO SOFTWARE

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
0700	31 00 02	0190	LD	SP,0200H	LOAD STACK POINTER
0703	ED 46	0200	IM	0	SET INTERRUPT MODE 0
0705		0210 *			(8080 IDENTICAL)
0705	FB	0220	EI		ENABLE INTERRUPTS
0706	3A B0 0A	0230	LD	A,(DECK)	
0709	F6 B0	0240	OR	0B0H	CONVERT TO ASCII
070B	32 83 07	0250	LD	(DKNFR),A	LOAD DECK # IN MESSAGE
070E	21 6E 07	0260	LD	HL,MSG1	
0711	CD 02 02	0270	CALL	TVEDIT	CALL TV EDITOR
0714	CD A8 01	0280 KYBD	CALL	01ASH	CALL KEYBOARD
0717	FE BA	0290	CP	0BAH	NUMBER?
0719	D2 38 07	0300	JP	NC,LET1	IF NO
071C	FE B0	0310	CP	0B0H	NUMBER?
071E	DA 4A 07	0320	JP	C,CHAR	NC
0721	F5	0330	PUSH	AF	SAVE A&F
0722	CD E6 00	0340	CALL	ERASE	ERASE SCREEN
0725	F1	0350	POP	AF	RESTORE A&F
0726	07	0360	RLCA		PRODUCE L INDEX
0727	D6 09	0370	SUB	09H	
0729	0F	0380	LD	L,A	
072A	26 07	0390 HINDEX	LD	H,07H	F INDEX
072C	7E	0400	LD	A,(HL)	SELECT ADDRESS
072D	32 36 07	0410	LD	(0736H),A	
0730	23	0420	INC	HL	
0731	7E	0430	LD	A,(HL)	
0732	32 37 07	0440	LD	(0737H),A	
0735	C3 00 00	0450	JP	SELADR	
0738	F6 20	0460 LETTER	OR	20H	
073A	FE F3	0470	CP	0F3H	"S" ?
073C	CA 00 03	0480	JP	Z,TVDUMP	YES, JUMP TO TV
073F		0490 *			STORAGE DUMP
073F	FE F2	0500	CP	0F2H	"R" ?
0741	CA 03 05	0510	JP	Z,0503H	YES, JUMP TO Z80 OPS SYSTEM
0744	FE F0	0520	CP	0F0H	"P" ?
0746	CA 91 24	0530	JP	Z,0491H	YES, JUMP TO KEYBOARD
0749		0540 *			PROGRAMMER ROUTINE
0749	CF	0550	RST	8D	
074A	FE A3	0560 CHAR	CP	0A3H	
074C	C2 14 07	0570	JP	NZ,KYBD	
074F	2E 6C	0580	LD	L,6CH	
0751	C3 2A 07	0590	JP	HINDEX	
0754	00	0600	NOP		
0755	00	0610	NOP		
0756	00	0620	NOP		

0757 00	2630	NCP	
0758 AD 08	2640	DW	08ADH 0 SELECT ADDRESS
075A D8 08	2650	DW	08D8H 1 SELECT ADDRESS
075C D2 08	2660	DW	08D2H 2 SELECT ADDRESS
075E CC 08	2670	DW	08CCH 3 SELECT ADDRESS
0760 DE 08	2680	DW	08DEH 4 SELECT ADDRESS
0762 E4 08	2690	DW	08E4H 5 SELECT ADDRESS
0764 EA 08	2700	DW	08EAH 6 SELECT ADDRESS
0766 F0 08	2710	DW	08F0H 7 SELECT ADDRESS
0768 F6 08	2720	DW	08F6H 8 SELECT ADDRESS
076A BF 08	2730	DW	08BFH 9 SELECT ADDRESS
076C 80 08	2740	DW	0880H # SELECT ADDRESS
076E FF	2750	DF	0FFH ERASE
076F	2760	DW	'# SET DECK'
A3 A0 D3 C5 CC			
A0 C4 C5 C3 CE			
0779 04	0770	DB	4D SPACES
077A	0780	DW	'IN USE - '
C9 CE A0 D5 D3			
C5 A0 AD A0			
0783	0790	DKNER	'0'
B0			
0784 08	0800	DF	8D SPACES
0785	0810	DW	'0 COPY TAPE'
B0 A0 C3 CF D0			
D9 A0 D4 C1 D0			
C5			
790 15	0820	DB	21D SPACES
0791	0830	DW	'1 ERASE'
B1 A0 C5 D2 C1			
D3 C5			
0798 19	0840	DF	25D SPACES
0799	0850	DW	'2 FAST REVERSE'
B2 A0 C6 C1 D3			
D4 A0 D2 C5 L6			
C5 D2 D3 C5			
07A7 12	0860	DB	18D SPACES
07A8	0870	DW	'3 FAST FORWARD'
B3 A0 C6 C1 D3			
D4 A0 C6 CF D2			
D7 C1 L2 C4			
07B6 12	0880	DB	18D SPACES
07E7	0890	DW	'4 STANDBY'
B4 A0 D3 D4 C1			
CE C4 C2 D9			
07C0 17	0900	DB	23D SPACES
07C1	0910	DW	'5 STOP'
B5 A0 D3 D4 CF			
D0			
07C7 1A	0920	DB	26D SPACES
07C8	0930	DW	'6 READ'
B6 A0 D2 C5 C1			
C4			
07CE 1A	0940	DB	26D SPACES
07CF	0950	DW	'7 RECORD'

B7 A0 D2 C5 C3				
CF D2 C4				
07D7 18	0960	DF	24D	SPACES
07D8	0970	DW	'8	RECORD TEST DATA'
B8 A0 D2 C5 C3				
CF D2 C4 A0 D4				
C5 D3 D4 A0 C4				
C1 D4 C1				
07EA 0E	0980	DF	14D	SPACES
07EB	0990	DW	'9	READ TEST DATA'
E9 A0 D2 C5 C1				
C4 A0 D4 C5 D3				
D4 A0 C4 C1 D4				
C1				
07FB 57	1000	DF	87D	SPACES
07FC	1010	DW	'PHI	DECK COMMANDS'
D0 C8 C9 A0 C4				
C5 C3 CB A0 C3				
CF CD CD C1 CE				
C4 D3				
080D 00	1020	DF	0D	RETURN
080E FF	1030	IB	0FFH	ERASE
080F 07	1040	DB	7D	SPACES
0810	1050	DW	'TAPE	BEING COPIED'
D4 C1 D0 C5 A0				
C2 C5 C9 CE C7				
A0 C3 CF D0 C9				
C5 C4				
0821 00	1060	DB	0D	RETURN
0822 FF	1070	LF	0FFH	ERASE
0823 06	1080	DB	6D	SPACES
0824	1090	DW	'RECORDING	TEST DATA'
D2 C5 C3 CF D2				
C4 C9 CE C7 A0				
D4 C5 D3 D4 A0				
C4 C1 D4 C1				
0837 00	1100	LB	0D	RETURN
0838 FF	1110	DF	0FFH	ERASE
0839 06	1120	DF	6D	SPACES
083A	1130	DW	'TEST	DATA BEING READ'
D4 C5 D3 D4 A0				
C4 C1 D4 C1 A0				
C2 C5 C9 CE C7				
A0 D2 C5 C1 C4				
084E 06	1140	DB	6D	SPACES
084F 00	1150	DF	0D	RETURN
0850 FF	1160	DF	0FFH	ERASE
0851	1170	DW	'SELECT	DECK NUMBER (0-3)'
D3 C5 CC C5 C3				
D4 A0 C4 C5 C3				
CB A0 CE D5 CD				
C2 C5 D2 A0 A8				
B0 AD B3 A9				
0869 28	1180	DF	40D	SPACES
086A	1190	DW	'DECK	#'

C4 C5 C3 CE A0				
A3 A0				
0871	1200	DNER	DW	'0'
B0				
0872 38	1210		DE	56D SPACES
2873	1220		DW	'DONE? (Y?)'
C4 CF CE C5 BF				
A0 A8 D9 BF A9				
087D 02	1230		DE	0D RETURN
087E 00	1240		NOP	
087F 00	1250		NOP	
0880 21 50 08	1260	TV	LD	HL,MSG5 LOAD H&L WITH DECK
0883	1270	*		SELECT MESSAGE
0883 3A B0 0A	1280		LD	A,(DECK) LOAD A WITH DECK #
0886 F6 F0	1290		OR	0F2H CONVERT TO ASCII
0888 32 71 0E	1300		LD	(DNER),A LOAD DECK NUMBER IN
088B	1310	*		MESSAGE AREA
088F CD 00 02	1320		CALL	TVEDIT CALL TV EDITOR
088E DB 00	1330	IN	IN	0 INPUT FROM KEYBOARD
0890 FE B4	1340		CP	0B4H >"3" ?
0892 D2 A5 08	1350		JP	NC,DONE YES, CHECK FOR "Y"
0895 FE B0	1360		CP	0B2E <"0" ?
0897 DA 8E 08	1370		JP	C,IN YES, JUMP TO KEYBOARD
089A	1380	*		(LOOK FOR A NUMBER)
089A 32 83 07	1390		LD	(DKNER),A IF BETWEEN 0 & 3, LOAD
089D	1400	*		DECK NUMBER IN MESSAGE
089D E6 03	1410		AND	3D MASK ALL BUT 3 LSP'S
089F 32 B0 0A	1420		LD	(DECK),A LOAD DECK NUMBER AT "DECK"
08A2 C3 80 08	1430		JP	TV DISPLAY MESSAGE WITH NEW DECK #
08A5 F6 20	1440	DONE	OR	20H CONVERT TO LOWER CASE
08A7 FE F9	1450		CP	0F9H "Y" ?
08A9 C2 80 0E	1460		JP	NZ,TV NO, JUMP TO MESSAGE
08AC CF	1470		RST	8D RESTART AT PHI_DECK
08AD	1480	*		COMMANDS IF "Y"
08AD 21 0E 08	1490	CPYTP	LD	HL,MSG2 LOAD H&L WITH MESSAGE AREA
08B0 CD 00 02	1500		CALL	TVEDIT CALL TV EDITOR
08B3 C3 C8 08	1510		JP	CPY JUMP TO COPY TAPE ROUTINE
08B6 21 22 08	1520	RCTD	LD	HL,MSG3 LOAD H&L WITH MESSAGE AREA
08B9 CD 00 02	1530		CALL	TVEDIT CALL TV EDITOR
08BC C3 A0 0B	1540		JP	RCDTD JUMP TO RECCRD TEST DATA
08BF	1550	*		ROUTINE
08BF 21 38 08	1560	RDTD	LD	HL,MSG4 LOAD H&L WITH MESSAGE AREA
08C2 CD 00 02	1570		CALL	TVEDIT CALL TV EDITOR
08C5 C3 CC 0B	1580		JP	RTD JUMP TO READ TEST DATA
08C8	1590	*		ROUTINE
08C8 CD 00 0C	1600	CPY	CALL	COPY CALL COPY TAPE ROUTINE
08CB CF	1610		RST	8D RESTART
08CC 0E A0	1620	FFWD	LD	C,0A0H LOAD C WITH FAST FORWARD
08CE	1630	*		COMMAND
08CE CD 9B 0A	1640		CALL	CMDOUT OUTPUT COMMAND
08D1 CF	1650		RST	8D RESTART
08D2 0E 80	1660	FREV	LD	C,80H LOAD C WITH FAST REVERSE
08D4	1670	*		COMMAND
08D4 CD 9B 0A	1680		CALL	CMDOUT OUTPUT COMMAND
08D7 CF	1690		RST	8D RESTART

08D8 0E EC	1700 ERASET LD C,0ECH	LOAD C WITH ERASE COMMAND
08DA CD 9E 0A	1710 CALL CMDOUT	OUTPUT COMMAND
08DD CF	1720 RST 8D	RESTART
08DE 0E 70	1730 STNDEY LD C,70H	LOAD C WITH STANDBY COMMAND
08E0 CD 9E 0A	1740 CALL CMDOUT	OUTPUT COMMAND
08E3 CF	1750 RST 8D	RESTART
08E4 0E F0	1760 STOP LD C,0F0H	LOAD C WITH STOP COMMAND
08E6 CD 9E 0A	1770 CALL CMDOUT	OUIPUT COMMAND
08E9 CF	1780 RST 8D	RESTART
08EA 0E E0	1790 READ LD C,0E0H	LOAD C WITH READ COMMAND
08EC CD 9E 0A	1800 CALL CMDOUT	OUTPUT COMMAND
08EF CF	1810 RST 8D	RESTART
08F0 0E E8	1820 RECORD LD C,0E8H	LOAD C WITH RECORD COMMAND
08F2 CD 9E 0A	1830 CALL CMDOUT	OUTPUT COMMAND
08F5 CF	1840 RST 8D	RESTART

0BA0	06	00	0100	RCDTD	LD	E,0D	INITIALIZE COUNT
0BA2	0E	08	0110		LD	C,0E2H	LOAD C WITH RECORD COMMAND
0BA4	CD	9F	0120		CALL	CMDOUT	OUTPUT COMMAND
0BA7	48		0130	RCD	LD	C,B	LOAD C WITH COUNT
0BAS	CD	AE	0140		CALL	DOUT	OUTPUT DATA
0BAP	DE	02	0150	STATUS	IN	2D	INPUT STATUS
0BAD	EC	03	0160		AND	3D	READY?
0BAF	CA	AB	0170		JP	Z,STATUS	NO, CHECK STATUS
0BB2	05		0180		DEC	B	DECREMENT COUNT
0BB3	C2	A7	0190		JP	NZ,RCD	256?
0BFC	16	02	0200		LD	D,2D	YES, OUTPUT DUMMY CHARACTERS
0BB6	4E		0210	LOOP	LD	C,B	
0BB9	CD	AE	0220		CALL	DOUT	
0BFC	DE	02	0230	STAT	IN	2D	INPUT STATUS
0BFE	E6	03	0240		AND	3D	READY?
0FC0	CA	BC	0250		JP	Z,STAT	NO, CHECK STATUS
0FC3	15		0260		DEC	D	DECREMENT LOOP
0FC4	C2	BE	0270		JP	NZ,LOOP	
0FC7	C3	A0	0280		JP	RCDTD	RECORD NEXT BLOCK
0ECA	00		0290		NOP		
0BCB	00		0300		NOP		
0BCC	06	02	0310	RTD	LD	E,0	INITIALIZE COUNT
0BCE	0E	00	0320		LD	C,0E2H	LOAD C WITH READ COMMAND
0BD0	CD	9B	0330		CALL	CMDOUT	OUTPUT COMMAND
0BD3	DE	02	0340	STATR	IN	2D	INPUT STATUS
0BD5	E6	03	0350		AND	3D	READY?
0BD7	CA	13	0360		JP	Z,STATR	NO, CHECK STATUS
0BDA	CD	8F	0370		CALL	DIN	YES INPUT DATA
0BD	79		0380		LD	A,C	LOAD A WITH DATA
0BDE	18		0390		CP	F	COMPARE TO COUNT
0BDF	C2	FF	0400		JP	NZ,ERROR	
0BE2	05		0410		DEC	B	DECREMENT COUNT
0BE3	C2	D3	0420		JP	NZ,STATR	
0BE6	21	FA	0430		LD	HL,GOOD	OUTPUT "G" IF BLOCK IS GOOD
0BE9	CD	00	0440		CALL	TVEDIT	CALL TV EDITOR
0BEC	C3	CC	0450		JP	RTD	READ NEXT BLOCK
0BEF	21	FE	0460	ERROR	LD	HL,ERR	OUTPUT "E" IF BLOCK IS
0BF2			0470	*			IN ERROR
0BF2	CD	02	0480		CALL	TVEDIT	CALL TV EDITOR
0BF5	C3	CC	0490		JP	RTD	READ NEXT BLOCK
0BF8	EE		0500	ERR	DP	0E0E	
0BFC	02		0510		DP	0	RETURN
0BFA	F7		0520	GOOD	DP	0E7E	
0BFB	20		0530		DP	0	RETURN
0BFC	00		0540		NOP		
0BFD	00		0550		NOP		
0BFE	00		0560		NOP		
0BFF	00		0570		NOP		
0C02	3E	02	0580	COPY	LD	A,2	SET DECK 2
0C02	32	EA	0590		LD	(DECK),A	STORE DECK 2
0C05	0F	0A	0600		CALL	REWIND	REWIND DECK 2
0C08	3E	01	0610		LD	A,1F	SET DECK 1
0C0A	32	EA	0620		LD	(DECK),A	STORE DECK 1

0C0D	CD	4F	0A	0630	CALL	REWIND	REWIND	DECK	1	
0C10	97			0640	SUP	A	CLEAR	A		
0C11	32	76	0C	0650	LD	(TEMPID),A	INITIALIZE	ID		
0C14	DB	02		0660	REDBLK	IN	TAPEIN			
0C16	EE	08		0670	AND	8D	WAIT	FOR	NOT	BUSY
0C18	CA	14	0C	0680	JP	Z,REDBLK				
0C1B	3E	00		0690	LD	A,0	SET	DECK	0	
0C1D	32	B0	0A	0700	LD	(DECK),A	STORE	DECK	0	
0C20	21	00	0D	0710	LD	HL,BUFFER	SET	UP	POINTER	
0C23	22	B3	0A	0720	LD	(POINTR),HL	POINTER	ADDRESS		
0C26	3A	76	0C	0730	LD	A,(TEMPID)	SET	UP	ID	
0C29	32	B1	2A	0740	LD	(IDR),A				
0C2C	1E	00		0750	LD	E,0	SET	UP	READ	MODE
0C2E	CD	E9	2A	0760	CALL	READ				
0C31	F5			0770	PUSH	AF	SAVE	A	&	FLAGS
0C32	0E	F0		0780	LD	C,0F0F	STOP	DECK		
0C34	CD	9B	0A	0790	CALL	CMDOUT				
0C37	F1			0800	POP	AF	RESTORE	A	&	FLAGS
0C38	FE	00		0810	CP	0	ERROR?			
0C3A	CA	41	0C	0820	JP	Z,WRTBLK	NO			
0C3D	FE	02		0830	CP	2D	BLOCK	FOUND?		
0C3F	C8			0840	RET	Z	NO,	FINISHED		
0C40	76			0850	HALT		HALT	BECAUSE	OF	ERROR
0C41	DB	02		0860	WRTBLK	IN	TAPEIN			
0C43	EE	08		0870	AND	8D	WAIT	FOR	NOT	BUSY
0C45	CA	41	0C	0880	JP	Z,WRTBLK				
0C48	3E	01		0890	LD	A,1D	SET	DECK	1	
0C4A	32	B0	2A	0900	LD	(DECK),A	STORE	DECK	1	
0C4D	21	00	0D	0910	LD	HL,BUFFER	SET	UP	POINTER	
0C50	22	B7	2A	0920	LD	(POINTW),HL				
0C53	3A	76	0C	0930	LD	A,(TEMPID)	SET	UP	ID	
0C56	32	B5	0A	0940	LD	(IDW),A				
0C59	3C			0950	INC	A				
0C5A	32	76	0C	0960	LD	(TEMPID),A				
0C5D	78			0970	LD	A,B	SET	UP	COUNT	
0C5E	FE	00		0980	CP	0	256?			
0C60	CA	69	0C	0990	JP	Z,X256				
0C63	68			1000	LD	L,B				
0C64	26	00		1010	LD	H,0				
0C66	C3	6D	0C	1020	JP	CALRCD				
0C69	26	01		1030	X256	LD	H,1D			
0C6B	2E	00		1040	LD	L,0				
0C6D	CD	00	09	1050	CALRCD	CALL	RECORD			
0C70	FE	00		1060	CP	0				
0C72	CA	14	0C	1070	JP	Z,REDBLK				
0C75	76			1080	HALT					

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<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
2902		2120	*	RECORD (UNTIL COUNT EXHAUSTED)	
2902		2110	*	DECK IS STOPPED AFTER RETURN	
2902		2120	*	INPUT:	
2902		2132	*	DECK - DECK NUMBER LOCATED IN MEMORY	
2902		2140	*	PCINTW - LOCATED IN MEMORY	
2902		2150	*	(FIRST DATA BYTE)	
2902		2162	*	IDW - LOCATED IN MEMORY (FIRST BLOCK)	
2902		2170	*	COUNT - REGISTER R,L	
2902		2182	*	OUTPUT:	
2902		2192	*	PCINTW - LOCATED IN MEMORY	
2902		2202	*	(LAST DATA BYTE + 1)	
2902		2210	*	ERRCR - REGISTER A	
2902		2220	*	2 - NO ERRORS	
2902		2232	*	1 - CRC ERROR IN BLOCK	
2902		2242	*	IDW - 1	
2902		2250	*	2 - BLOCK IDW-1 NOT FOUND	
2902		2260	*	3 - TAPE END OR JAM	
2902		2272	*	IDW - LOCATED IN MEMORY	
2902		2282	*	(LAST BLOCK + 1)	
2902		2292	*	ALTERED	
2902		2320	*	REGISTERS - A,R,C,D,E,H,L,IDR,POINTR	
2902	16	2310	RECORD	LI I,11	ERASE=1
2902	1E	2320		LD E,5D	STOPS=5
2904	E5	2332		PUSH HL	COUNT
2905	1E	2342	RCD20	PUSH DE	ERASE, STOPS
2906	2A	2352		LD HL,(IDW)	
2909	2F	2362		DEC HL	IDR=IDW -1
290A	27	2372		LL (IDR),HL	
290D	23	2380		INC HL	
290E	71	2392		LD A,L	IDW=0 ?
290F	B4	2402		OR H	
2910	CA	2412		JP Z,RCD10	YES
2913	16	2422		LL D,11D	RETRIEFS = 12
2915	1E	2432		LD E,1D	CHECK MODE
2917	CD	2442		CALL ALTRD	
291A	3C	2452		INC A	ERRCR?
291F	31	2462		DEC A	
291C	CA	2472		JP Z,RCD13	NO
291F	11	2482	RCD12	POP DE	ERASE, STOPS
2920	E1	2492	RCD21	POP HL	COUNT
2921	2E	2502	RCD27	LD C,90H	STOP
2923	47	2512		LD F,A	SAVE ERROR
2924	CF	2522		CALL CMDOUT	
2927	7E	2532		LD A,B	RESTORE ERROR
292F	09	2542		RET	
2939	CF	2552	RCD10	CALL REWIND	
2940	4E	2562		LD C,0ECE	ERASE
2941	CF	2572		CALL CMDOUT	

0931	3E	28	0580	LD	A,40D	4 SECONDS
0933	CD	81 0A	0590	CALL	DELAY	
0936	D1		0600	POP	DE	ERASE, STOPS
0937	D5		0610	PUSH	DE	
0938	15		0620	DEC	D	ERASE (ERASE - 1) BLOCKS
0939	CA	49 09	0630	JP	Z,RCD14	
093C	0E	EC	0640	LD	C,0ECC	ERASE
093E	CD	9B 0A	0650	CALL	CMDOUT	
0941	D5		0660	PUSH	DE	
0942	CD	DA 09	0670	CALL	RECRD1	
0945	I1		0680	FOP	DE	
0946	C3	38 09	0690	JP	RCD15	
0949	E1		0700	POP	HL	ERASE, STOPS
094A	D1		0710	POP	DE	COUNT
094B	D5		0720	PUSH	DE	
094C	E5		0730	PUSH	HL	
094D	2A	B7 2A	0740	LD	HL,(POINTW) POINTER	
0950	15		0750	DEC	D	COUNT HIGH = 0?
0951	14		0760	INC	D	
0952	C2	D4 09	0770	JP	NZ,RCD16	NO
0955	1D		0780	DEC	E	
0956	1C		0790	INC	E	
0957	CA	81 09	0800	JP	Z,RCD17	YES
095A	43		0810	LD	B,E	COUNT = COUNTL
095B	1E	00	0820	LD	E,0D	COUNTL = 0
095D	D5		0830	PUSH	DE	SAVE COUNT
095E	EB		0840	EX	TE,HL	
095F	2A	B1 0A	0850	LD	HL,(IDR)	
0962	23		0860	INC	HL	
0963	22	B1 0A	0870	LD	(IDR),HL	
0966	EB		0880	EX	DE,HL	
0967	0E	E8	0890	LD	C,0E8H	RECORD
0969	CD	9B 2A	0900	CALL	CMDOUT	
096C	CD	DA 09	0910	CALL	RECRD1	
096F	DF	02	0920	IN	TAPEIN	ERROR?
0971	E6	0D	0930	AND	0DH	
0973	D1		0940	POP	DE	GET COUNT
0974	CA	52 09	0950	JP	Z,RCD19	NO
0977	I1		0960	POP	DE	DECREMENT STOPS
0978	1D		0970	DEC	E	0?
0979	C2	05 09	0980	JP	NZ,RCD20	NO
097C	3E	03	0990	LD	A,3D	ERROR=3
097E	C3	20 09	1000	JP	RCD21	
0981	3E	05	1010	LD	A,5D	APPROXIMATELY 10 BLOCKS
0983	CD	68 0A	1020	CALL	FR	
0986	E1		1030	POP	HL	ERASE, STOPS
0987	D1		1040	POP	DE	COUNT
098E	D5		1050	PUSH	DE	
0989	E5		1060	PUSH	HL	
098A	97		1070	SUB	A	COUNT=0?
098B	E2		1080	ADD	D	
098C	C2	93 09	1090	JP	NZ,RCD22	NO
098F	83		1100	ADD	E	
0990	CA	1F 09	1110	JP	Z,RCD12	YES
0993	2A	B5 0A	1120	LD	HL,(IDW)	
0996	22	B1 0A	1130	LD	(IDR),HL	

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0999 16 06          1140      LD    L,6D    RETRIES = 6
099P 1E 01          1150      LD    E,1D    CHECK MODE
099L CL BB 0A      1160      CALL ALTRT2
09A0 3C            1170      INC  A        ERROR?
09A1 3D            1180      DEC  A
09A2 D1            1190      POP  IE
09A3 CA AA 00      1200      JP   Z,RCD24 NO
09A5 14            1210      INC  D        INCREMENT FRASE
09A7 C3 25 29      1220      JP   RCD20
09AA 10 21          1230      LD    D,1D    ERASE=1
09AC 2A 50 2A      1240      LD    HL,(IDW) INCREMENT IDW
09AF 23            1250      INC  HL
09B2 22 20 2A      1260      LD    (IDW),HL
09E3 EF            1270      EX  DE,HI
09E4 11            1280      POP  IE
09E5 14            1290      INC  D        COUNT# =27
09E6 15            1300      DEC  D
09B7 CA C7 29      1310      JP   Z,RCD21 YES
09BA 15            1320      DEC  D        DECREMENT COUNT#
09EE E5            1330      PUSH HL
09EC 2A B7 2A      1340      LD    HL,(POINTW)
09EF 24            1350      INC  F
09C0 22 B7 2A      1360      LD    (POINTW),HL
09C3 E1            1370      POP  HL
09C4 C3 80 29      1380      JP   RCD26
09C7 2A F7 2A      1390      LD    HL,(POINTW) ALL COUNCIL TO POINTER
09CA 16 00          1400      LD    I,27
09CC 19            1410      ADD  HL,DE
09CD 22 B7 2A      1420      LD    (POINTW),HL
09D0 07            1430      SUB  A        ERROR = 2
09D1 C3 21 29      1440      JP   RCD27
09D4 15            1450      DEC  D        DECREMENT COUNT#
09I5 20 00          1460      LD    E,0F    COUNT#0
09D7 C3 50 29      1470      JP   RCD18
09DA 1450 * RECD1 (RECORD ONE BLOCK)
09LA 1490 * RECD1 OR ERASE COMMAND MUST BE ISSUED
09DA 1500 * BEFORE CALLING.
09DA 1510 * UNDERRUN AND STOP SHOULD BE CHECKED
09DA 1520 * AFTER RETURN.
09DA 1540 * INPUTS:
09IA 1550 * DECK - DECK NUMBER LOCATED
09IA 1560 * IN MEMORY
09DA 1570 * ID - REGISTER I, F
09IA 1580 * (COUNT - REGISTER F
09IA 1600 * (01=1 BYTE, 00=256 BYTES)
09DA 1610 * POINTER - REGISTER E, I
09DA 1620 * (FIRST DATA BYTE)
09IA 1630 * OUTPUT:
09DA 1640 * POINTER - REGISTER E, I
09DA 1650 * (LAST DATA BYTE + 1)
09DA 1660 * ALIBREL
09DA 1670 * REGISTERS - A, B, C, D, E, H, L
09IA E5 RECD1 PUSH HL PUSH POINTW
09EB 21 22 00      1680      LD    HL,21  RECD1=0
09DE 4A            1700      LD    C,D    IS=100
09DF CD 40 0A      1710      CALL ALIBUT

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09E2	4B		1720	LD	C,E	ID LOW
09E3	CD	42 0A	1730	CALL	PUT	
09E6	4B		1740	LD	C,B	COUNT
09E7	CD	42 0A	1750	CALL	PUT	
09EA	54		1760	ID	D,H	SAVE CRC2
09EB	4L		1770	LD	C,L	CRC1
09EC	CD	42 0A	1780	CALL	PUT	
09EF	4A		1790	LD	C,D	CRC2
09F0	CD	42 0A	1800	CALL	PUT	
09F3	5B		1810	LD	E,B	SAVE COUNT
09F4	E3		1820	EX	(SP),HL	SWITCH CRC, POINTER
09F5	4E		1830	LD	C,(HL)	LOAD DATA
09F6	23		1840	INC	HL	INCREMENT POINTER
09F7	E3		1850	EX	(SP),HL	SWITCH CRC, POINTER
09F8	CD	42 2A	1860	CALL	PUT	
09FF	05		1870	DEC	B	DECREMENT COUNT
09FC	C2	F4 09	1880	JP	NZ,RECD1	NOT ZERO
09FF	54		1890	LD	D,H	SAVE CRC2
0A00	4D		1900	LD	C,L	CRC1
0A01	CD	42 0A	1910	CALL	PUT	
0A04	4A		1920	LD	C,D	CRC2
0A05	CD	42 0A	1930	CALL	PUT	
0A08	1D		1940	DEC	E	DECREMENT SAVED COUNT
0A09	CD	42 2A	1950	CALL	PUT	
0A0C	1C		1960	INC	E	INCREMENT SAVED COUNT
0A0D	C2	09 0A	1970	JP	NZ,RECD3	NCT ZERO
0A10	CD	42 0A	1980	CALL	PUT	
0A13	E1		1990	POP	HL	POP POINTER
0A14	C9		2000	RET		
0A15			2010	*	GET	
0A15			2020	*	CRC IN H,L	
0A15			2030	*	DATA RETURNED IN C	
0A15			2040	*	A,C,H,L ALTERED	
0A15	DB	02	2050	GET	IN	TAPEIN STATUS
0A17	E6	0F	2060	AND	0FH	
0A19	CA	15 2A	2070	JP	Z,GET	
0A1C	CD	8F 0A	2080	CALL	DIN	
0A1F	D5		2090	CRC	PUSH	DE
0A20	79		2100	LD	A,C	
0A21	AD		2110	XOR	L	
0A22	6F		2120	LD	L,A	
0A23	1E	07	2130	LD	E,7D	7 TIMES
0A25	17		2140	CRCA	RLA	A
0A26	AD		2150	XOR	L	
0A27	1D		2160	DEC	E	
0A28	C2	25 0A	2170	JP	NZ,CRCA	DONE?
0A2B	6F		2180	LD	L,A	YES
0A2C	0F		2190	RRCA	A	
0A2D	0F		2200	RRCA	A	
0A2E	5F		2210	LD	E,A	SAVE 1
0A2F	E6	C0	2220	AND	0C0H	
0A31	AC		2230	XOR	H	
0A32	57		2240	LD	D,A	SAVE 2
0A33	7B		2250	LD	A,E	RESTORE 1
0A34	E6	3F	2260	AND	3FH	
0A36	AD		2270	XOR	L	

0A37	67	2282	LD	E,A	CRC HIGH DONE	
0A38	17	2292	RLA	A	TEST BIT 7	
0A39	7A	2302	LD	A,D	RESTORE 2	
0A3A	D2 3F 0A	2312	JP	NC,CRCFIN	BIT 7 WAS 1?	
0A3D	EE 21	2322	XCR	1D	YES	
0A3F	6F	2332	CRCFIN	LD	L,A	CRC LOW DONE
0A40	D1	2342	POP	DF		
0A41	C9	2352	RFT			
0A42		2362	*	PUT		
0A42		2372	*	DATA IN REGISTER C		
0A42		2382	*	CRC IN H,L		
0A42		2392	*	A,H,L ALTERED		
0A42	DF 02	2402	PUT	IN	TAPEIN STATUS	
0A44	EE 2F	2412	AND	0FH		
0A46	CA 42 0A	2422	JP	Z,PUT		
0A49	CD A8 0A	2432	ALTPUT	CALL	DOUT	
0A4C	C3 1F 0A	2442	JP	CRC		
0A4F		2452	*	REWIND		
0A4F		2462	*	REGISTER A,C ALTERED		
0A4F		2472	*	THIS ROUTINE WILL GUARANTEE		
0A4F		2482	*	LECK SELECTION		
0A4F	0E 92	2492	REWIND	LD	C,90H	STOP
0A51	CD 91 0A	2502		CALL	CMDOUT	
0A54	DB 22	2512	REWB	IN	TAPEIN	
0A56	EE 08	2522		AND	08H	
0A58	CA 54 0A	2532		JP	Z,REWF	
0A5F	0E 82	2542		LD	C,80H	FR
0A5D	CD 9E 0A	2552		CALL	CMDOUT	
0A62	DF 22	2562	REWA	IN	TAPEIN	
0A62	EE 08	2572		AND	ED	
0A64	CA 62 0A	2582		JP	Z,REWA	
0A67	C9	2592		RET		
0A68		2602	*	FAST REVERSE, FAST FORWARD		
0A68		2612	*	REGISTER A CONTAINS MULTIPLE		
0A68		2622	*	CF 100 MILLI-SECONDS DELAY		
0A68		2632	*	REGISTER A ALTERED		
0A68	C5	2642	FR	PUSH	BC	
0A69	F5	2652		PUSH	AF	
0A6A	0E 82	2662		LD	C,80H	
0A6C	CD 9E 0A	2672	FRA	CALL	CMDOUT	
0A6F	F1	2682		POP	AF	
0A72	CD 81 0A	2692		CALL	DELAY	
0A73	0E 92	2702		LD	C,90H	
0A75	CD 9E 0A	2712		CALL	CMDOUT	
0A78	C1	2722		POP	BC	
0A79	C9	2732		RET		
0A7A	C5	2742	FF	PUSH	BC	
0A7B	F5	2752		PUSH	AF	
0A7C	0E A2	2762		LD	C,0A0H	
0A7E	C3 6C 0A	2772		JP	FRA	
0A81		2782	*	DELAY MULTIPLE OF 100 MS IN REGISTER A		
0A81		2792	*	REGISTERS A,B,C ALTERED		
0A81	01 E4 29	2802	DELAY	LD	EC,29B4H	
0A84	0B	2812	D1	DEC	BC	
A85	04	2822		INC	B	
0A86	05	2832		DEC	B	

0A87	C2	84	0A	2840	JP	NZ,D1
0A8A	3D			2850	DEC	A
0A8B	C2	81	0A	2860	JP	NZ,DELAY
0A8E	C9			2870	RET	
0A8F				2880	*	INPUT DATA BYTE (DATA RETURNED IN C)
0A8F				2890	*	REGISTER A IS ALTERED
0A8F	3E	EF		2900	DIN	LD A,2EFE
0A91	D3	01		2910	OUT	STROBE
0A93	LB	02		2920	IN	TAPEIN
0A95	4F			2930	LD	C,A
0A96	3E	DF		2940	DINA	LD A,0DFH
0A98	L3	01		2950	OUT	STROBE
0A9A	C9			2960	RET	
0A9F				2970	*	OUTPUT COMMAND (DATA IN REGISTER C)
0A9F				2980	*	DECK IS OR'D WITH DATA
0A9B				2990	*	REGISTER A IS ALTERED
0A9E	3A	E2	0A	3000	CMDCUT	LD A,(DECK)
0A9E	E1			3010	OR	C
0A9F	D3	02		3020	OUT	TAPOUT
0AA1	3E	9F		3030	LD	A,9FH
0AA3	D3	01		3040	CMDA	CUT STROBE
0AA5	C3	96	0A	3050	JP	DINA
0AA8				3060	*	OUTPUT DATA (DATA IN REGISTER C)
0AA8				3070	*	REGISTER A IS ALTERED
0AA8	79			3080	DOUT	LD A,C
0AA9	D3	02		3090	OUT	TAPOUT
0AAE	3E	5F		3100	LD	A,5FH
0AAD	C3	A3	0A	3110	JP	CMDA
0AB0				3120	*	VARIABLE DATA AREA
0AB0				3130	DECK	DS 1D DECK NUMBER TO BE USED
0AB1				3140	IDR	DS 2D READ ID
0AB3				3150	POINTR	DS 2D READ POINTER
0AB5				3160	IDW	DS 2D WRITE IL
0AB7				3170	POINTW	DS 2D WRITE POINTER
0AB9				3180	*	READ ONE FLOCK
0AB9				3190	*	DECK REMAINS RUNNING AFTER RETURN
0AB9				3200	*	INPUT:
0AB9				3210	*	DECK - DECK NUMBER LOCATED IN MEMORY
0AB9				3220	*	POINTR - LOCATED IN MEMORY
0AB9				3230	*	(FIRST BYTE)
0AB9				3240	*	IDR - LOCATED IN MEMORY
0AB9				3250	*	RETRYS - REGISTER D
0AB9				3260	*	(ALTRD ONLY)
0AB9				3270	*	MODE - REGISTER E
0AB9				3280	*	0=READ
0AB9				3290	*	1=CHECK
0AB9				3300	*	OUTPUT:
0AB9				3310	*	DECK, POINTER, IDR UNCHANGED
0AB9				3320	*	REGISTER - A,B,C,D,H,L ALTERED
0AB9				3330	*	COUNT - REGISTER E
0AB9				3340	*	01=1 BYTE
0AB9				3350	*	00=256 BYTES
0AB9				3360	*	ERROR - REGISTER A
0AB9				3370	*	0=NO ERRORS
0AB9				3380	*	1=CRC ERROR
0AB9				3390	*	2=BLOCK NOT FOUND

0AB9		3400	*		3=END OF TAPE OR JAM
0AB9		3410	*	ENTRY POINTS:	
0AB9		3420	*	READ - NORMAL ENTRY	
0AB9		3430	*	ALTRD - DECK WILL BACKSPACE	
0AB9		3440	*	FIRST, USER MUST SUPPLY RETRIES	
0AB9		3450	*	ALTRD2 - NORMAL, EXCEPT USER MUST	
0AB9		3460	*	SUPPLY RETRIES.	
0AF9	16 0A	3470	READ	LD D,10D	RETRIES
0AEB	D5	3480	RD54	PUSH DE	RETRIES, MODE
0AFC		3490	ALTRD2	EQU RD54	
0ABC	21 00 00	3500	RD5	LD HL,0D	RESET CRC
0ABF	DB 02	3510		IN TAPEIN	STATUS
0AC1	57	3520		LD D,A	
0AC2	0E E0	3530	RD51	LD C,0E0H	READ
0AC4	CD 9B 0A	3540		CALL CMDOUT	
0AC7	7A	3550		LD A,D	STOP?
0ACE	E6 04	3560		AND 04H	
0ACA	CA D7 0A	3570		JP Z,RD50	NO
0ACD	3E 04	3580		LD A,4D	.4 SECONDS
0ACF	CD 81 0A	3590		CALL DELAY	
0AD2	16 00	3600		LD D,0D	STATUS=0
0AD4	C3 C2 0A	3610		JP RD51	
0AD7	06 3A	3620	RD50	LD B,3AH	8 SECOND TIMEOUT
0AD9	50	3630	RD57	LD D,B	
0ADA	DE 02	3640	RD53	IN TAPEIN	STATUS
0ADC	E6 0F	3650		AND 0FH	READY?
0ADE	C2 90 0B	3660		JP NZ,RD10	YES
0AE1	1F	3670		DEC DE	
0AE2	14	3680		INC D	
0AE3	15	3690		DEC D	
0AE4	C2 DA 0A	3700		JP NZ,RD53	
0AE7	05	3710		DEC B	
0AE8	C2 D9 0A	3720		JP NZ,RD57	
0AEP	CD 4F 0A	3730		CALL REWIND	
0AEE	3E 02	3740	RD2	LD A,2D	ERROR=2
0AF0	D1	3750		POP DE	RETRIES, MODE
0AF1	15	3760	RD8	DEC D	
0AF2	C2 BB 0A	3770		JP NZ,RD54	
0AF5	C9	3780		RET	
0AF6	CD 15 0A	3790	RD52	CALL GET	IDH
0AF9	41	3800		LD B,C	
0AFA	CD 15 0A	3810		CALL GET	IDL
0AFD	59	3820		LD E,C	
0AFE	CD 15 0A	3830		CALL GET	COUNT
0B01	51	3840		LD D,C	
0B02	CD 15 0A	3850		CALL GET	CRC1
0B05	CD 15 0A	3860		CALL GET	CRC2
0B08	97	3870		SUB A	CRC=0?
0B09	84	3880		ADD H	
0B0A	C2 BC 0A	3890		JP NZ,RD5	NO
0B0D	85	3900		ADD L	
0E0E	C2 EC 0A	3910		JP NZ,RD5	NO
0B11		3920	*	COMPUTE	BE TAPEID
0B11		3930	*		-HL IDR
0E11		3940	*		=XY
0B11	7B	3950		LD A,E	

2B12	2A	F1	2A	3960	LI	HL,(ITP)	
2B15	95			3972	SUB	I	
2B16	5F			3984	LD	E,A	REGISTER 1 CONTAINS Y
2B17	6F			3997	IF	L,A	
2B18	7E			4000	LI	A,H	
2B19	9C			4012	SEC	F	REGISTER A CONTAINS Y
2B1A	67			4024	IF	E,A	F=XY/F
2B1B	29			4032	ADD	HL,HL	
2B1C	29			4042	ADD	HL,FI	
2B1D	29			4052	ADD	HL,FI	
2B1E	29			4062	ADD	HL,FI	
2B1F	29			4070	ADD	HL,FI	
2B22	7C			4082	LI	A,H	
2B21	CA	38	2F	4090	JP	Z,IT1	
2B24	F2	3D	0E	4100	JP	P,ID2	
2B27	2F			4110	CPL		COMPUTE FF DELAY
2B28	C6	02		4120	ADD	2D	ADD1+1 FOR 2'S COMP
2B2A	FA	32	0E	4130	JP	M,ID3	
2B2D	FE	04		4142	CF	4D	GREATER THAN THRESHOLD?
2B2F	FA	BC	0A	4152	JP	M,RI5	NO
2B32	CD	7A	2A	4160	CALL	FF	
2B35	C3	EC	2A	4170	JP	RDS	
2B38	1C			4180	INC	E	Y=0?
2B39	1D			4190	DEC	E	
2B3A	CA	45	2F	4200	JP	Z,RDS	YES
2B3D	C6	06		4210	APL	6D	
2B3F	CD	68	2A	4220	CALL	FR	
2B42	C3	EE	0A	4230	JP	RD2	
2B45	42			4240	LD	B,D	COUNT
2B46	D1			4250	POP	DE	RETRIES, MODE
2B47	C5			4260	PUSH	FC	CCUNT
2B48	2A	B3	2A	4270	LD	HL,(POINIR)	
2B4B	E5			4280	PUSH	FL	
2B4C	21	02	00	4290	LD	HL,2D	RESET CRC
2B4F	CF	15	2A	4300	CALL	GET	
2B52	1C			4310	INC	E	
2B53	1D			4320	DEC	E	
2B54	C2	5F	0B	4330	JP	NZ,RI56	
2B57	E3			4340	EX	(SP),HL	SWITCH CRC, POINTER
2B58	71			4350	LD	(HL),C	STORE DATA
2B59	23			4360	INC	HL	BUMP POINTER
2B5A	E3			4370	EX	(SP),HL	SWITCH CRC, POINTER
2B5E	05			4380	DEC	E	DECREMENT COUNT
2B5C	C2	4F	0B	4390	JP	NZ,RD56	
2B5F	C1			4400	POP	FC	ADJUST STACK POINTER
2B60	C1			4410	POP	FC	CCUNT
2B61	CD	15	2A	4420	CALL	GET	
2B64	CD	15	2A	4430	CALL	GET	
2B67	DE	02		4440	IN	TAPEIN	STATUS
2B69	1F			4450	RRA		OVERRUN?
2B6A	DA	7B	0B	4460	JP	C,ALTRD	YES
2B6D	1F			4470	RRA	A	
2B6E	1F			4480	RRA	A	STOP?
2B6F	DA	96	0B	4490	JP	C,RD11	YES
2B72	97			4500	SUB	A	
2B73	E4			4510	ADD	H	

0B74	C2	7F	0P	4520	JP	NZ,ALTRD	NO
0E77	85			4530	ADD	L	
0B78	CA	85	0B	4540	JP	Z,RD19	
0B7B	3E	05		4550	ALTRD	LD	A,5D GREATER THAN 1 BLOCK
0B7D	CD	6E	0A	4560	CALL	FR	
0B80	3E	01		4570	LD	A,1D	ERROR=1
0B82	C3	F1	0A	4580	JP	RDE	
0B85	50			4590	RD19	LL	I,B SAVE COUNT
0B86	15			4600	DEC	D	DECREMENT SAVED COUNT
0B87	CD	15	0A	4610	RD9	CALL	GET
0B8A	14			4620	INC	D	INCREMENT SAVED COUNT
0B8B	C2	87	0B	4630	JP	NZ,RD9	
0B8E	97			4640	SUB	A	ERROR=0
0B8F	C9			4650	RET		
0B90	EE	04		4660	RD10	AND	04H STOP?
0B92	CA	F6	2A	4670	JP	Z,RD52	NO
0B95	I1			4680	POP	DE	RETRIES, MODE
0B96	CD	4F	0A	4690	RD11	CALL	REWIND
0B99	3E	03		4700	LT	A,3D	ERROR=3
2B9B	C3	F1	0A	4710	JP	RDE	

8080 PHI-DECK DEMO SOFTWARE

1. Programs are loaded via AUDIO CASSETTE.
2. At completion of a successful load, a listing of Phi-Deck Command options will be displayed.
3. In addition to the options displayed on the screen, there are also three options possible - "R", "S", and "P".
4. "R" will return control to 8080 OPS System options which include:
 - 1 READ Cassette - Read an Audio Cassette
 - 2 WRITE Cassette - Write an Audio Cassette
 - 3 TV Storage Dump - TV Display of Memory in Octal
 - 4 Keyboard Program - User may program in Octal
 - 5 PHI-DECK OPS
5. "S" will display memory as option 3 in 8080 OPS System.
6. "P" will allow user to program same as option 4 in 8080 OPS System.
7. Reset will return control to Phi-Deck Commands.
8. "P", "R", and "S" will operate also when in Program, Storage Dump, or Phi-Deck OPS.
9. Phi-Deck Option "#" allows user to select any of four decks (0-3) by first pressing shift and # then the desired deck number. To return to Phi-Deck OPS press Y. The deck number selected will be displayed in Options listing upon return.
10. Phi-Deck Option "1" will erase a tape on the selected deck.
11. Phi-Deck Option "2" will fast reverse the selected deck.
12. Phi-Deck Option "3" will fast forward the selected deck.
13. Phi-Deck Option "4" will place all decks in standby. The capstan motors will be turned off.
14. Phi-Deck Option "5" will stop the selected deck.
15. Phi-Deck Option "6" will issue a read command to the selected deck. This will not read data from the tape.
16. Phi-Deck Option "7" will issue a record command to the selected deck. This will not record data on the tape.
17. Phi-Deck Option "8" will record 256 byte blocks of data in a fixed pattern.
18. Phi-Deck Option "9" will read 256 byte blocks of data in the same pattern as recorded in Option "8". An "e" will be displayed on the monitor for blocks in error and a "g" for good blocks.
19. Page 015 is being used as a 256 byte buffer in the copy tape routine.
20. Option "0" will copy a tape from deck #0 to deck #1. This is not intended as an efficient method of duplicating Phi-Deck Tapes, only as a demonstration of Phi-Deck routines.

CHANGES TO 8080 OPERATING SYSTEM
FOR PHI-DECK DEMO

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
005 112	170				ADDRESS JUMP FOR KEY 5
005 113	007				
005 271	016				SPACES 5
005 272	265				
005 273	240				P H I D E C K O P S RETURN
005 274	320				
005 275	310				
005 276	311				
005 277	240				
005 300	304				
005 301	305				
005 302	303				
005 303	313				
005 304	240				
005 305	317				
005 306	320				
005 307	323				
005 310	000				
001 003	170				
001 004	007				
003 257	003				
003 260	005				
004 176	003				
004 177	005				
005 000	303				
005 001	170				
005 002	007				

8080 PHI-DECK DEMO SOFTWARE

LOC	OBJ	LABEL	OP	OPERAND	COMMENTS
007 000	076 000	COPY	MVI	A, 0	SET DECK 0
007 002	062 260 012		STA	DECK	STORE DECK #
007 005	315 117 012		CALL	REWIND	REWIND DECK 0
007 010	076 001		MVI	A,1	SET DECK 1
007 012	062 260 012		STA	DECK	STORE DECK #
007 015	315 117 012		CALL	REWIND	REWIND DECK 1
007 020	227		SUB	A	CLEAR A
007 021	062 166 007		STA	TEMPID	INITIALIZE ID
007 024	333 002	REDBLK	IN	TAPEIN	WAIT FOR NOT BUSY
007 026	346 010		ANI	010	
007 030	312 024 007		JZ	REDBLK	
007 033	076 000		MVI	A,0	SET DECK 0
007 035	062 260 012		STA	DECK	STORE DECK #
007 040	041 000 015		LXI	H,BUFFER	SET UP POINTER
007 043	042 263 012		SHLD	POINTR	STORE POINTER ADDRESS
007 046	072 166 007		LDA	TEMPID	SET UP ID
007 051	062 261 012		STA	IDR	
007 054	036 000		MVI	E,0	SET UP READ MODE
007 056	315 271 012		CALL	READ	READ A BLOCK
007 061	365		PUSH	PSW	SAVE A
007 062	016 360		MVI	C, 360	STOP DECK
007 064	315 233 012		CALL	CMDOUT	
007 067	361		POP	PSW	RESTORE A
007 070	376 000		CPI	0	ERROR
007 072	312 101 007		JZ	WRTBLK	NO
007 075	376 002		CPI	002	BLOCK FOUND?
007 077	310		RZ		NO, FINISHEE
007 100	166		HLT		HALT BECAUSE OF ERROR
007 101	333 002	WRTBLK	IN	TAPEIN	WAIT FOR NOT BUSY DECK NUMBER CHANGING
007 103	346 010		ANI	010	
007 105	312 101 007		JZ	WRTBLK	
007 110	076 001		MVI	A,1	SET DECK 1
007 112	062 260 012		STA	DECK	
007 115	041 000 015		LXI	H,BUFFER	SET UP POINTER
007 120	042 267 012		SHLD	POINTW	
007 123	072 166 007		LDA	TEMPID	SET UP ID
007 126	062 265 012		STA	IDW	
007 131	074		INR	A	INCREMENT ID
007 132	062 166 007		STA	TEMPID	
007 135	170		MOV	A,B	SET UP COUNT
007 136	376 000		CPI	0	256?
007 140	312 151 007		JZ	X256	
007 143	150		MOV	L,B	

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
007 144	046 000		MVI	H,0	
007 146	303 155 007		JMP	CALRCD	
007 151	046 001	X256	MVI	H,1	
007 153	056 000		MVI	L,0	
007 155	315 000 011	CALRCD	CALL	RECORD	RECORD BLOCK
007 160	376 000		CPI	0	
007 162	312 024 007		JZ	REDBLK	
007 165	166		HLT		
007 166	000 000	TEMPID			
007 170	061 000 002		LXI	SP	LOAD STACK POINTER
007 173	373		EI		
007 174	041 316 007		LXI	H	
007 177	072 260 012		LDA	(012 260)	LOAD A W DECK #
007 202	366 260		ORI	260	CONVERT TO ASCII
007 204	062 342 007		STA	007 342	PLACE DECK # IN MESSAGE
007 207	315 045 002		CALL	TVEDIT	CALL TV EDITOR
007 212	315 000 002	KYBD	CALL		CALL KEYBOARD
007 215	376 272		CPI	272	NUMBER?
007 217	322 155 010		JNC	LETTER	NO, JUMP TO LETTERS
007 222	376 260		CPI	260	< 0 ?
007 224	332 256 007		JC	CHARS	YES, JUMP TO CHARS
007 227	365		PUSH	A	SAVE A
007 230	315 021 002		CALL	ERASE	ERASE
007 233	361		POP	A	RESTORE A
007 234	007		RLC		ROTATE LEFT
007 235	306 127		ADI	127	PRODUCE L INDEX
007 237	157		MOV	L,A	
007 240	046 007		MVI	H, 007	H INDEX
007 242	176		MOV	A,M	
007 243	062 254 007		STA		STORE A
007 246	043		INX	H	INCREMENT H & L
007 247	176		MOV	A,M	
007 250	062 255 007		STA		
007 253	303 * *		JMP		
007 256	376 243	CHARS	CPI	243	# ?
007 260	302 212 007		JNZ	KYBD	
007 263	056 314		MVI	L, 314	
007 265	303 240 007		JMP		
007 270	300 013				0 SELECT ADDRESS
007 272	217 010				1 SELECT ADDRESS
007 274	211 010				2 SELECT ADDRESS
007 276	203 010				3 SELECT ADDRESS

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
007 300	225	010			4 SELECT ADDRESS
007 302	233	010			5 SELECT ADDRESS
007 304	241	010			6 SELECT ADDRESS
007 306	247	010			7 SELECT ADDRESS
007 310	311	013			8 SELECT ADDRESS
007 312	322	013			9 SELECT ADDRESS
007 314	115	014			# SELECT ADDRESS
007 316	377				ERASE
007 317	243				#
007 320	240				
007 321	323				S
007 322	345				e
007 323	354				l
007 324	240				
007 325	304				D
007 326	345				e
007 327	343				c
007 330	353				k
007 331	004				SPACES
007 332	311				I
007 333	356				n
007 334	240				
007 335	325				U
007 336	363				s
007 337	345				e
007 340	240				
007 341	240				
007 342	260				Ø
007 343	011				SPACES
007 344	260				Ø
007 345	240				
007 346	303				C
007 347	357				o
007 350	360				p
007 351	371				y
007 352	240				
007 353	324				T
007 354	341				a
007 355	360				p
007 356	345				e
007 357	025				SPACES
007 360	261				l
007 361	240				

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
007 362	305				E
007 363	362				r
007 364	341				a
007 365	363				s
007 366	345				e
007 367	031				SPACES
007 370	262				2
007 371	240				
007 372	306				F
007 373	341				a
007 374	363				s
007 375	364				t
007 376	240				
007 377	322				R
010 000	345				e
010 001	366				v
010 002	345				e
010 003	362				r
010 004	363				s
010 005	345				e
010 006	022				SPACES
010 007	263				3
010 010	240				
010 011	306				F
010 012	341				a
010 013	363				s
010 014	364				t
010 015	240				
010 016	306				F
010 017	357				o
010 020	362				r
010 021	367				w
010 022	341				a
010 023	362				r
010 024	344				d
010 025	022				SPACES
010 026	264				4
010 027	240				
010 030	323				S
010 031	364				t
010 032	341				a
010 033	356				n
010 034	344				d
010 035	342				b
010 036	371				y
010 037	027				SPACES

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
Ø1Ø Ø4Ø	265				5
Ø1Ø Ø41	24Ø				
Ø1Ø Ø42	323				S
Ø1Ø Ø43	364				t
Ø1Ø Ø44	357				o
Ø1Ø Ø45	36Ø				p
Ø1Ø Ø46	Ø32				SPACES
Ø1Ø Ø47	266				6
Ø1Ø Ø5Ø	24Ø				
Ø1Ø Ø51	322				R
Ø1Ø Ø52	345				e
Ø1Ø Ø53	341				a
Ø1Ø Ø54	344				d
Ø1Ø Ø55	Ø32				SPACES
Ø1Ø Ø56	267				7
Ø1Ø Ø57	24Ø				
Ø1Ø Ø6Ø	322				R
Ø1Ø Ø61	345				e
Ø1Ø Ø62	343				c
Ø1Ø Ø63	357				o
Ø1Ø Ø64	362				r
Ø1Ø Ø65	344				d
Ø1Ø Ø66	Ø3Ø				SPACES
Ø1Ø Ø67	27Ø				8
Ø1Ø Ø7Ø	24Ø				
Ø1Ø Ø71	322				R
Ø1Ø Ø72	345				e
Ø1Ø Ø73	343				c
Ø1Ø Ø74	357				o
Ø1Ø Ø75	362				r
Ø1Ø Ø76	344				d
Ø1Ø Ø77	24Ø				
Ø1Ø 1ØØ	324				T
Ø1Ø 1Ø1	345				e
Ø1Ø 1Ø2	363				s
Ø1Ø 1Ø3	364				t
Ø1Ø 1Ø4	24Ø				
Ø1Ø 1Ø5	3Ø4				D
Ø1Ø 1Ø6	341				a
Ø1Ø 1Ø7	364				t
Ø1Ø 11Ø	341				a
Ø1Ø 111	Ø16				SPACES
Ø1Ø 112	271				9
Ø1Ø 113	24Ø				
Ø1Ø 114	322				R

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
Ø1Ø 115	345				e
Ø1Ø 116	341				a
Ø1Ø 117	344				d
Ø1Ø 12Ø	24Ø				
Ø1Ø 121	324				T
Ø1Ø 122	345				e
Ø1Ø 123	363				s
Ø1Ø 124	364				t
Ø1Ø 125	24Ø				
Ø1Ø 126	3Ø4				D
Ø1Ø 127	341				a
Ø1Ø 13Ø	364				t
Ø1Ø 131	341				a
Ø1Ø 132	127				SPACES
Ø1Ø 133	32Ø				P
Ø1Ø 134	31Ø				H
Ø1Ø 135	311				I
Ø1Ø 136	24Ø				
Ø1Ø 137	3Ø4				D
Ø1Ø 14Ø	3Ø5				E
Ø1Ø 141	3Ø3				C
Ø1Ø 142	313				K
Ø1Ø 143	24Ø				
Ø1Ø 144	3Ø3				C
Ø1Ø 145	317				O
Ø1Ø 146	315				M
Ø1Ø 147	315				M
Ø1Ø 15Ø	3Ø1				A
Ø1Ø 151	316				N
Ø1Ø 152	3Ø4				D
Ø1Ø 153	323				S
Ø1Ø 154	ØØØ				RETURN
Ø1Ø 155	366 Ø4Ø	LETTER	ORI	Ø4Ø	PRODUCE LOWER CASE
Ø1Ø 157	376 363		CPI	363	'S' ?
Ø1Ø 161	312 ØØØ ØØ3		JZ	ØØ3 ØØØ	JUMP IF 'S' TO STORAGE DUMP
Ø1Ø 164	376 362		CPI	362	'R' ?
Ø1Ø 166	312 ØØ3 ØØ5		JZ	ØØ5 ØØ3	JUMP IF EQUAL TO 8Ø8Ø OPS SYSTEM
Ø1Ø 171	376 36Ø		CPI	36Ø	'P' ?
Ø1Ø 173	312 Ø65 ØØ4		JZ	ØØ4 Ø65	JUMP IF EQUAL TO KEYBOARD PROGRAMMING
Ø1Ø 176	317		RST	Ø1Ø	
Ø1Ø 177	315 ØØØ ØØ7	CPY	CALL	COPY	COPY TAPE ROUTINE

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
Ø1Ø 2Ø2	317		RST	Ø1Ø	RESTART
Ø1Ø 2Ø3	Ø16 24Ø	FFWD	MVI	C, 24Ø	LOAD C w FAST FORWARD
Ø1Ø 2Ø5	315 233 Ø12		CALL	CMDOUT	OUTPUT COMMAND
Ø1Ø 21Ø	317		RST	Ø1Ø	RESTART
Ø1Ø 211	Ø16 2ØØ	FREV	MVI	C, 2ØØ	LOAD C w FAST REVERSE
Ø1Ø 213	315 233 Ø12		CALL	CMDOUT	OUTPUT COMMAND
Ø1Ø 216	317		RST	Ø1Ø	RESTART
Ø1Ø 217	Ø16 354	ERASE	MVI	C, 354	LOAD C w ERASE
Ø1Ø 221	315 233 Ø12		CALL	CMDOUT	OUTPUT COMMAND
Ø1Ø 224	317		RST	Ø1Ø	RESTART
Ø1Ø 225	Ø16 16Ø	STNDBY	MVI	C, 16Ø	LOAD C w STANDBY
Ø1Ø 227	315 233 Ø12		CALL	CMDOUT	OUTPUT COMMAND
Ø1Ø 232	317		RST	Ø1Ø	RESTART
Ø1Ø 233	Ø16 36Ø	STOP	MVI	C, 36Ø	LOAD C w STOP
Ø1Ø 235	315 233 Ø12		CALL	CMDOUT	OUTPUT COMMAND
Ø1Ø 24Ø	317		RST	Ø1Ø	RESTART
Ø1Ø 241	Ø16 34Ø	READ	MVI	C, 34Ø	LOAD C w READ
Ø1Ø 243	315 233 Ø12		CALL	CMDOUT	OUTPUT COMMAND
Ø1Ø 246	317		RST	Ø1Ø	RESTART
Ø1Ø 247	Ø16 35Ø	RECORD	MVI	C, 35Ø	LOAD C w RECORD
Ø1Ø 251	315 233 Ø12		CALL	CMDOUT	OUTPUT COMMAND
Ø1Ø 254	317		RST	Ø1Ø	RESTART
Ø1Ø 26Ø	ØØ6 ØØØ	RCDTD	MVI	B, Ø	INITIALIZE COUNT
Ø1Ø 262	Ø16 35Ø		MVI	C, 35Ø	LOAD C w RECORD
Ø1Ø 264	315 233 Ø12		CALL	CMDOUT	OUTPUT COMMAND
Ø1Ø 267	11Ø	RCD	MOV	C, B	LOAD C w COUNT
Ø1Ø 27Ø	315 25Ø Ø12		CALL	DOUT	OUTPUT DATA
Ø1Ø 273	333 ØØ2	STATUS	IN	2	INPUT STATUS
Ø1Ø 275	346 ØØ3		ANI	3	READY
Ø1Ø 277	312 273 Ø1Ø		JZ	STATUS	NO, INPUT STATUS
Ø1Ø 3Ø2	ØØ5		DEC	B	YES, DECREMENT COUNT
Ø1Ø 3Ø3	3Ø2 267 Ø1Ø		JNZ	RCD	256?
Ø1Ø 3Ø6	Ø26 ØØ2		MVI	D, 2	YES, OUTPUT ADDED CHARACTERS TO ALLOW TIME FOR DELAY
Ø1Ø 31Ø	11Ø	LOOP	MOV	C,B	LOAD C w COUNT
Ø1Ø 311	315 25Ø Ø12		CALL	DOUT	OUTPUT DATA
Ø1Ø 314	333 ØØ2	STAT	IN	2	INPUT STATUS
Ø1Ø 316	346 ØØ3		ANI	3	READY?
Ø1Ø 32Ø	312 314 Ø1Ø		JZ	STAT	NO, INPUT STATUS

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
Ø1Ø 323	Ø25		DEC	D	YES, DECREMENT LOOP COUNT
Ø1Ø 324	3Ø2 31Ø Ø1Ø		JNZ	LOOP	
Ø1Ø 327	3Ø3 26Ø Ø1Ø		JMP	RCDTD	RECORD NEXT BLOCK
Ø1Ø 334	ØØ6 ØØØ	RTD	MVI	B, Ø	INITIALIZE COUNT
Ø1Ø 336	Ø16 34Ø		MVI	C, 340	LOAD C w READ
Ø1Ø 34Ø	315 233 Ø12		CALL	CMDOUT	OUTPUT COMMAND
Ø1Ø 343	333 ØØ2	STATR	IN	2	INPUT STATUS
Ø1Ø 345	346 ØØ3		ANI	3	READY?
Ø1Ø 347	312 343 Ø1Ø		JZ	STATR	NO
Ø1Ø 352	315 217 Ø12		CALL	DIN	YES, INPUT DATA
Ø1Ø 355	171		MOV	A,C	MOVE DATA TO A
Ø1Ø 356	27Ø		CMP	B	COMPARE TO COUNT
Ø1Ø 357	3Ø2 262 Ø13		JNZ	ERROR	JUMP IF NOT EQUAL TO ERROR
Ø1Ø 362	ØØ5		DEC	B	DECREMENT COUNT
Ø1Ø 363	3Ø2 343 Ø1Ø		JNZ	STATR	256? NO, READ NEXT BYTE
Ø1Ø 366	Ø41 275 Ø13		LXI	H	OUTPUT 'g' IF END OF BLOCK
Ø1Ø 371	315 Ø45 ØØ2		CALL	TVEDIT	CALL TV EDITOR
Ø1Ø 374	3Ø3 334 Ø1Ø		JMP	RTD	READ NEXT BLOCK

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
Ø13 262	Ø41 273 Ø13	ERROR	LXI	H	OUTPUT 'e' IF ERROR
Ø13 265	315 Ø45 ØØ2		CALL	TVEDIT	CALL TV EDITOR
Ø13 27Ø	3Ø3 334 Ø1Ø		JMP	RTD	READ NEXT BLOCK
Ø13 273	345		DB	345	'e'
Ø13 274	ØØØ		DB	Ø	RETURN
Ø13 275	347		DB	347	'g'
Ø13 276	ØØØ		DB	Ø	RETURN
Ø13 3ØØ	Ø41 335 Ø13		LXI	H	LOAD COPY TAPE MESSAGE AREA
Ø13 3Ø3	315 Ø45 ØØ2		CALL	TVEDIT	CALL TV EDITOR
Ø13 3Ø6	3Ø3 177 Ø1Ø		JMP	CPY	JUMP TO COPY TAPE ROUTINE
Ø13 311	Ø41 361 Ø13		LXI	H	LOAD RECORDING TEST DATA MESSAGE AREA
Ø13 314	315 Ø45 ØØ2		CALL	TVEDIT	CALL TV EDITOR
Ø13 317	3Ø3 26Ø Ø1Ø		JMP	RCDTD	JUMP TO RECORD TEST DATA ROUTINE
Ø13 322	Ø41 ØØ7 Ø14		LXI	H	LOAD READ TEST DATA MESSAGE AREA
Ø13 325	315 Ø45 ØØ2		CALL	TVEDIT	CALL TV EDITOR
Ø13 33Ø	3Ø3 334 Ø1Ø		JMP	RTD	JUMP TO READ TEST DATA ROUTINE
Ø13 335	377				ERASE
Ø13 336	ØØ7				SPACES
Ø13 337	324				T
Ø13 34Ø	341				a
Ø13 341	36Ø				p
Ø13 342	345				e
Ø13 343	24Ø				
Ø13 344	3Ø2				B
Ø13 345	345				e
Ø13 346	351				i
Ø13 347	356				n
Ø13 35Ø	347				g
Ø13 351	24Ø				
Ø13 352	3Ø3				C
Ø13 353	357				o
Ø13 354	36Ø				p
Ø13 355	351				i
Ø13 356	345				e
Ø13 357	344				d
Ø13 36Ø	ØØØ				RETURN
Ø13 361	377				ERASE
Ø13 362	ØØ6				SPACES

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
Ø13 363	322				R
Ø13 364	345				e
Ø13 365	343				c
Ø13 366	357				o
Ø13 367	362				r
Ø13 37Ø	344				d
Ø13 371	351				i
Ø13 372	356				n
Ø13 373	347				g
Ø13 374	24Ø				
Ø13 375	324				T
Ø13 376	345				e
Ø13 377	363				s
Ø14 ØØØ	364				t
Ø14 ØØ1	24Ø				
Ø14 ØØ2	3Ø4				D
Ø14 ØØ3	341				a
Ø14 ØØ4	364				t
Ø14 ØØ5	341				a
Ø14 ØØ6	ØØØ				RETURN
Ø14 ØØ7	377				ERASE
Ø14 Ø1Ø	ØØ6				SPACES
Ø14 Ø11	324				T
Ø14 Ø12	345				e
Ø14 Ø13	363				s
Ø14 Ø14	364				t
Ø14 Ø15	24Ø				
Ø14 Ø16	3Ø4				D
Ø14 Ø17	341				a
Ø14 Ø2Ø	364				t
Ø14 Ø21	341				a
Ø14 Ø22	24Ø				
Ø14 Ø23	3Ø2				B
Ø14 Ø24	345				e
Ø14 Ø25	351				i
Ø14 Ø26	356				n
Ø14 Ø27	347				g
Ø14 Ø3Ø	24Ø				
Ø14 Ø31	322				R
Ø14 Ø32	345				e
Ø14 Ø33	341				a
Ø14 Ø34	344				d
Ø14 Ø35	ØØ6				SPACES

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
Ø14 Ø36	ØØØ				RETURN
Ø14 Ø37	377				ERASE
Ø14 Ø4Ø	323				S
Ø14 Ø41	345				e
Ø14 Ø42	354				l
Ø14 Ø43	345				e
Ø14 Ø44	343				c
Ø14 Ø45	364				t
Ø14 Ø46	24Ø				
Ø14 Ø47	3Ø4				D
Ø14 Ø5Ø	345				e
Ø14 Ø51	343				c
Ø14 Ø52	353				k
Ø14 Ø53	24Ø				
Ø14 Ø54	316				N
Ø14 Ø55	365				u
Ø14 Ø56	355				m
Ø14 Ø57	342				b
Ø14 Ø6Ø	345				e
Ø14 Ø61	362				r
Ø14 Ø62	24Ø				
Ø14 Ø63	25Ø				(
Ø14 Ø64	26Ø				Ø
Ø14 Ø65	255				-
Ø14 Ø66	263				3
Ø14 Ø67	251)
Ø14 Ø7Ø	Ø5Ø				SPACES
Ø14 Ø71	3Ø4				D
Ø14 Ø72	345				e
Ø14 Ø73	343				c
Ø14 Ø74	353				k
Ø14 Ø75	24Ø				
Ø14 Ø76	243				#
Ø14 Ø77	24Ø				
Ø14 1ØØ	26Ø				Ø
Ø14 1Ø1	Ø7Ø				SPACES
Ø14 1Ø2	3Ø4				D
Ø14 1Ø3	357				o
Ø14 1Ø4	356				n
Ø14 1Ø5	345				e
Ø14 1Ø6	277				?
Ø14 1Ø7	24Ø				
Ø14 11Ø	25Ø				(
Ø14 111	331				Y
Ø14 112	277				?

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
Ø14 113	251)
Ø14 114	ØØØ				RETURN
Ø14 115	Ø41 Ø37 Ø14	TV	LXI	H,Ø14 Ø37	LOAD H & L W MESSAGE AREA
Ø14 12Ø	Ø72 26Ø Ø12		LDA	DECK	LOAD A w DECK #
Ø14 123	366 26Ø		ORI	26Ø	CONVERT TO ASCII
Ø14 125	Ø62 1ØØ Ø14		STA	Ø14 1ØØ	STORE IN MESSAGE
Ø14 13Ø	315 Ø45 ØØ2		CALL	TVEDIT	CALL TV EDITOR
Ø14 133	333 ØØØ	IN	IN	Ø	INPUT FROM KEYBOARD
Ø14 135	376 264		CPI	264	> '3' ?
Ø14 137	322 162 Ø14		JPC	DONE	YES
Ø14 142	376 26Ø		CPI	26Ø	< 'Ø' ?
Ø14 144	332 133 Ø14		JPC	IN	YES
Ø14 147	Ø62 342 ØØ7		STA	ØØ7 342	PLACE NUMBER IN MESSAGE
Ø14 152	346 ØØ3		ANI	3	
Ø14 154	Ø62 26Ø Ø12		STA	DECK	STORE DECK #
Ø14 157	3Ø3 115 Ø14		JMP	TV	JUMP TO MESSAGE
Ø14 162	366 Ø4Ø	DONE	ORI	Ø4Ø	CONVERT TO LOWER CASE
Ø14 164	376 371		CPI	371	'y' ?
Ø14 16Ø	3Ø2 115 Ø14		JNZ	TV	NO
Ø14 171	317		RST	Ø1Ø	YES

8080 DRIVER SOFTWARE (HEX)

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
		*		RECORD (UNTIL COUNT EXHAUSTED)	
		*		DECK IS STOPPED AFTER RETURN	
		*		INPUT:	
		*		DECK - DECK NUMBER LOCATED IN MEMORY	
		*		POINTW - LOCATED IN MEMORY	
		*		(FIRST DATA BYTE)	
		*		IDW - LOCATED IN MEMORY (FIRST BLOCK)	
		*		COUNT - REGISTER H,L	
		*		OUTPUT:	
		*		POINTW - LOCATED IN MEMORY	
		*		(LAST DATA BYTE + 1)	
		*		ERROR - REGISTER A	
		*		0 - NO ERRORS	
		*		1 - CRC ERROR IN BLOCK	
		*		IDW - 1	
		*		2 - BLOCK IDW-1 NOT FOUND	
		*		3 - TAPE END OR JAM	
		*		IDW - LOCATED IN MEMORY	
		*		(LAST BLOCK + 1)	
		*		ALTERED	
		*		REGISTERS - A,B,C,D,E,H,L,IDR,POINTR	
0900	1601	RECORD	MVI	D,1	ERASE = 1
0902	1E05		MVI	E,5	STOPS = 5
0904	E5		PUSH	H	COUNT
0905	D5	RCD20	PUSH	D	ERASE, STOPS
0906	2AB50A		LHLD	IDW	
0909	2B		DCX	H	IDR = IDW - 1
090A	22B10A		SHLD	IDR	
090D	23		INX	H	
090E	7D		MOV	A,L	IDW = 0 ?
090F	B4		ORA	H	
0910	CA2909		JZ	RCD10	YES
0913	160B		MVI	D,11	RETRIES = 10
0915	1E01		MVI	E,1	CHECK MODE
0917	CD7B0B		CALL	ALTRD	
091A	3C		INR	A	ERROR?
091B	3D		DCR	A	
091C	CA3609		JZ	RCD13	NO
091F	D1	RCD12	POP	D	ERASE, STOPS
0920	E1	RCD21	POP	H	COUNT
0921	0E90	RCD27	MVI	C,90H	STOP
0923	47		MOV	B,A	SAVE ERROR
0924	CD9B0A		CALL	CMDOUT	
0927	78		MOV	A,B	RESTORE ERROR
0928	C9		RET		
0929	CD4F0A	RCD10	CALL	REWIND	
092C	0EEC		MVI	C,ECH	ERASE

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
Ø92E	CD9BØA		CALL	CMDOUT	
Ø931	3E28		MVI	A,40	4 SECONDS
Ø933	CD81ØA		CALL	DELAY	
Ø936	D1	RCD13	POP	D	ERASE, STOPS
Ø937	D5		PUSH	D	
Ø938	15	RCD15	DCR	D	ERASE (ERASE - 1) BLOCKS
Ø939	CA49Ø9		JZ	RCD14	
Ø93C	ØEEC		MVI	C,ECH	ERASE
Ø93E	CD9BØA		CALL	CMDOUT	
Ø941	D5		PUSH	D	
Ø942	CDDAØ9		CALL	RECRD1	
Ø945	D1		POP	D	
Ø946	C338Ø9		JMP	RCD15	
Ø949	Ø1	RCD14	POP	H	ERASE, STOPS
Ø94A	D1		POP	D	COUNT
Ø94B	D5		PUSH	D	
Ø94C	E5		PUSH	H	
Ø94D	2AB7ØA		LHLD	POINTW	POINTER
Ø950	15	RCD19	DCR	D	COUNT HIGH = Ø?
Ø951	14		INR	D	
Ø952	C2D4Ø9		JNZ	RCD16	NO
Ø955	1D		DCR	E	
Ø956	1C		INR	E	
Ø957	CA81Ø9		JZ	RCD17	YES
Ø95A	43		MOV	B,E	COUNT = COUNTL
Ø95B	1EØØ		MVI	E,Ø	COUNTL = Ø
Ø95D	D5	RCD18	PUSH	D	SAVE COUNT
Ø95E	EB		XCHG		
Ø95F	2AB1ØA		LHLD	IDR	
Ø962	23		INX	H	
Ø963	22B1ØA		SHLD	IDR	
Ø966	EB		XCHG		
Ø967	ØEE8		MVI	C,E8H	RECORD
Ø969	CD9BØA		CALL	CMDOUT	
Ø96C	CDDAØ9		CALL	RECRD1	
Ø96F	DBØ2		IN	TAPEIN	ERROR?
Ø971	E6ØD		ANI	ØDH	
Ø973	D1		POP	D	GET COUNT
Ø974	CA5ØØ9		JZ	RCD19	NO
Ø977	D1		POP	D	DCR STOPS
Ø978	1D		DCR	E	Ø?
Ø979	C2Ø5Ø9		JNZ	RCD20	NO
Ø97C	3EØ3		MVI	A,3	ERROR = 3
Ø97E	C32ØØ9		JMP	RCD21	
Ø981	3EØ5	RCD17	MVI	A,5	APPROXIMATELY 10 BLOCKS
Ø983	CD68ØA		CALL	FR	
Ø986	E1		POP	H	ERASE, STOPS
Ø987	D1		POP	D	COUNT
Ø988	D5	RCD26	PUSH	D	
Ø989	E5		PUSH	H	
Ø98A	97		SUB	A	COUNT = Ø?

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
Ø98B	82		ADD	D	
Ø98C	C293Ø9		JNZ	RCD22	NO
Ø98F	83		ADD	E	
Ø99Ø	CA1FØ9		JZ	RCD12	YES
Ø993	2AB5ØA	RCD22	LHLD	IDW	
Ø996	22B1ØA		SHLD	IDR	
Ø999	16Ø6		MVI	D,6	RETRIES = 6
Ø99B	1EØ1		MVI	E,1	CHECK MODE
Ø99D	CDBBØA		CALL	ALTRD2	
Ø9AØ	3C		INR	A	ERROR?
Ø9A1	3D		DCR	A	
Ø9A2	D1		POP	D	
Ø9A3	CAAAØ9		JZ	RCD24	NO
Ø9A6	14		INR	D	INCREMENT ERASE
Ø9A7	C3Ø5Ø9		JMP	RCD20	
Ø9AA	16Ø1	RCD24	MVI	D,1	ERASE = 1
Ø9AC	2AB5ØA		LHLD	IDW	INCREMENT IDW
Ø9AF	23		INX	H	
Ø9BØ	22B5ØA		SHLD	IDW	
Ø9B3	EB		XCHG		
Ø9B4	D1		POP	D	
Ø9B5	14		INR	D	COUNTH = Ø?
Ø9B6	15		DCR	D	
Ø9B7	CAC7Ø9		JZ	RCD25	YES
Ø9BA	15		DCR	D	DECREMENT COUNTH
Ø9BB	E5		PUSH	H	
Ø9BC	2AB7ØA		LHLD	POINTW	
Ø9BF	24		INR	H	
Ø9CØ	22B7ØA		SHLD	POINTW	
Ø9C3	E1		POP	H	
Ø9C4	C388Ø9		JMP	RCD26	
Ø9C7	2AB7ØA	RCD25	LHLD	POINTW	ADD COUNTL TO POINTER
Ø9CA	16ØØ		MVI	D,Ø	
Ø9CC	19		DAD	D	
Ø9CD	22B7ØA		SHLD	POINTW	
Ø9DØ	97		SUB	A	ERROR = Ø
Ø9D1	C321Ø9		JMP	RCD27	
Ø9D4	15	RCD16	DCR	D	DECREMENT COUNTH
Ø9D5	Ø6ØØ		MVI	B,Ø	COUNT = Ø
Ø9D7	C35DØ9		JMP	RCD18	

* RECRD1 (RECORD ONE BLOCK)

* RECORD OR ERASE COMMAND MUST BE ISSUED
* BEFORE CALLING.

* UNDERRUN AND STOP SHOULD BE CHECKED
* AFTER RETURN.

* INPUTS:

* DECK - DECK NUMBER LOCATED
* IN MEMORY

* ID - REGISTER D, E

* COUNT - REGISTER B

(Ø1=1 BYTE, ØØ=256 BYTES)

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
		*		POINTER - REGISTER H,L	
		*		(FIRST DATA BYTE)	
		*		OUTPUT:	
		*		POINTER - REGISTER H,L	
		*		(LAST DATA BYTE + 1)	
		*		ALTERED	
		*		REGISTERS - A,B,C,D,E,H,L	
Ø9DA	E5	RECD1	PUSH	H	PUSH POINTER
Ø9DB	21 ØØØØ		LXI	H,Ø	RESET CRC
Ø9DE	4A		MOV	C,D	ID HIGH
Ø9DF	CD 49ØA		CALL	ALTPUT	
Ø9E2	4B		MOV	C,E	ID LOW
Ø9E3	CD42ØA		CALL	PUT	
Ø9E6	48		MOV	C,B	COUNT
Ø9E7	CD42ØA		CALL	PUT	
Ø9EA	54		MOV	D,H	SAVE CRC2
Ø9EB	4D		MOV	C,L	CRC1
Ø9EC	CD42ØA		CALL	PUT	
Ø9EF	4A		MOV	C,D	CRC2
Ø9FØ	CD42ØA		CALL	PUT	
Ø9F3	58		MOV	E,B	SAVE COUNT
Ø9F4	E3	RECD1	XTHL		SWITCH CRC, POINTER
Ø9F5	4E		MOV	C,M	LOAD DATA
Ø9F6	23		INX	H	INCREMENT POINTER
Ø9F7	E3		XTHL		SWITCH CRC, POINTER
Ø9F8	CD42ØA		CALL	PUT	
Ø9FB	05		DCR	B	DECREMENT COUNT
Ø9FC	C2F4Ø9		JNZ	RECD1	NOT ZERO
Ø9FF	54		MOV	D,H	SAVE CRC2
ØAØØ	4D		MOV	C,L	CRC1
ØAØ1	CD42ØA		CALL	PUT	
ØAØ4	4A		MOV	C,D	CRC2
ØAØ5	CD42ØA		CALL	PUT	
ØAØ8	1D		DCR	E	DECREMENT SAVED COUNT
ØAØ9	CD42ØA	RECD3	CALL	PUT	
ØAØC	1C		INR	E	INCREMENT SAVED COUNT
ØAØD	C2Ø9ØA		JNZ	RECD3	NOT ZERO
ØA1Ø	CD42ØA		CALL	PUT	
ØA13	E1		POP	H	POP POINTER
ØA14	C9		RET		
		*	GET		
		*		CRC IN H,L	
		*		DATA RETURNED INC	
		*		A,C,H,L, ALTERED	
ØA15	DBØ2	GET	IN	TAPEIN	STATUS
ØA17	E6ØF		ANI	ØFH	
ØA19	CA15ØA		JZ	GET	
ØA1C	CD8FØA		CALL	DIN	
ØA1F	D5	CRC	PUSH	D	
ØA2Ø	79		MOV	A,C	
ØA21	AD		XRA	L	

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
ØA22	6F		MOV	L,A	
ØA23	1EØ7		MVI	E,7	007 TIMES
ØA25	17	CRCA	RAL		
ØA26	AD		XRA	L	
ØA27	1D		DCR	E	
ØA28	C225ØA		JNZ	CRCA	DONE?
ØA2B	6F		MOV	L,A	YES
ØA2C	ØF		RRC		
ØA2D	ØF		RRC		
ØA2E	5F		MOV	E,A	SAVE 1
ØA2F	E6CØ		ANI	CØH	
ØA31	AC		XRA	H	
ØA32	57		MOV	D,A	SAVE 2
ØA33	7B		MOV	A,E	RESTORE 1
ØA34	E63F		ANI	3FH	
ØA36	AD		XRA	L	
ØA37	67		MOV	H,A	CRC HIGH DONE
ØA38	17		RAL		TEST BIT 7
ØA39	7A		MOV	A,D	RESTORE 2
ØA3A	D23FØA		JNC	CRCFIN	BIT 7 WAS 1?
ØA3D	EEØ1		XRI	1	YES
ØA3F	6F	CRCFIN	MOV	L,A	CRC LOW DONE
ØA4Ø	D1		POP	D	
ØA41	C9		RET		
		*	PUT		
		*			DATA IN REGISTER C
		*			CRC IN H,L
		*			A,H,L ALTERED
ØA42	DBØ2	PUT	IN	TAPEIN	STATUS
ØA44	E6ØF		ANI	ØFH	
ØA46	CA42ØA		JZ	PUT	
ØA49	CDA8ØA	ALTPUT	CALL	DOUT	
ØA4C	C31FØA		JMP	CRC	
		*			REWIND
		*			REGISTER A, C ALTERED
		*			THIS ROUTINE WILL GUARANTEE
		*			DECK SELECTION
ØA4F	OE9Ø	REWIND	MVI	C,9ØH	STOP
ØA51	CD9BØA		CALL	CMDOUT	
ØA54	DBØ2	REWB	IN	TAPEIN	
ØA56	E6Ø8		ANI	O8H	
ØA58	CA54ØA		JZ	REWB	
ØA5B	OE8Ø		MVI	C,8ØH	FR
ØA5D	CD9BØA		CALL	CMDOUT	
ØA6Ø	DBØ2	REWA	IN	TAPEIN	
ØA62	E6Ø8		ANI	8	
ØA64	CA6ØØA		JZ	REWA	
ØA67	C9		RET		
		*			FAST REVERSE, FAST FORWARD
		*			REGISTER A CONTAINS MULTIPLE
		*			OF 100 MILLI-SECONDS DELAY
		*			REGISTER A ALTERED

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
ØA68	C5	FR	PUSH	B	
ØA69	F5		PUSH	PSW	
ØA6A	ØE80		MVI	C,80H	
ØA6C	CD9BØA	FRA	CALL	CMDOUT	
ØA6F	F1		POP	PSW	
ØA7Ø	CD81ØA		CALL	DELAY	
ØA73	ØE9Ø		MVI	C,90H	
ØA75	CD9BØA		CALL	CMDOUT	
ØA78	C1		POP	B	
ØA79	C9		RET		
ØA7A	C5	FF	PUSH	B	
ØA7B	F5		PUSH	PSW	
ØA7C	ØEAØ		MVI	C,AØH	
ØA7E	C36CØA		JMP	FRA	
		*	DELAY MULTIPLE OF 100 MS IN REGISTER A.		
		*	REGISTERS A,B,C ALTERED		
ØA81	O1002O	DELAY	LXI	B,2000H	
ØA84	OB	D1	DCX	B	
ØA85	O4		INR	B	
ØA86	O5		DCR	B	
ØA87	C284ØA		JNZ	D1	
ØA8A	3D		DCR	A	
ØA8B	C281ØA		JNZ	DELAY	
ØA8E	C9		RET		
		*	INPUT DATA BYTE (DATA RETURNED IN C)		
		*	REGISTER A IS ALTERED		
ØA8F	3EEF	DIN	MVI	A,EFH	
ØA91	D3O1		OUT	STROBE	
ØA93	DBO2		IN	TAPEIN	
ØA95	4F		MOV	C,A	
ØA96	3EDF	DINA	MVI	A,DFH	
ØA98	D3O1		OUT	STROBE	
ØA9A	C9		RET		
		*	OUTPUT COMMAND (DATA IN REGISTER C)		
		*	DECK IS OR'D WITH DATA		
		*	REGISTER A IS ALTERED		
ØA9B	3ABØØA	CMDOUT	LDA	DECK	
ØA9E	B1		ORA	C	
ØA9F	D3O2		OUT	TAPOUT	
ØAA1	3E9F		MVI	A,9FH	
ØAA3	D3O1	CMDA	OUT	STROBE	
ØAA5	C396ØA		JMP	DINA	
		*	OUTPUT DATA (DATA IN REGISTER C)		
		*	REGISTER A IS ALTERED		
ØAA8	79	DOUT	MOV	A,C	
ØAA9	D3O2		OUT	TAPOUT	
ØAAB	3E5F		MVI	A,5FH	
ØAAD	C3A3ØA		JMP	CMDA	
		*	VARIABLE DATA AREA		
ØABØ	OO	DECK	DS	1	DECK NUMBER TO BE USED
ØAB1	OO OO	IDR	DS	2	READ ID

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
ØAB3	00 00	POINTR	DS	2	READ POINTER
ØAB5	00 00	IDW	DS	2	WRITE ID
ØAB7	00 00	POINTW	DS	2	WRITE POINTER
		*	READ ONE BLOCK		
		*	DECK REMAINS RUNNING AFTER RETURN		
		*	INPUT:		
		*	DECK - DECK NUMBER LOCATED IN MEMORY		
		*	POINTR - LOCATED IN MEMORY		
		*	(FIRST BYTE)		
		*	IDR - LOCATED IN MEMORY		
		*	RETRYS - REGISTER D		
		*	(ALTRD ONLY)		
		*	MODE - REGISTER E		
		*	Ø=READ		
		*	1=CHECK		
		*	OUTPUT:		
		*	DECK, POINTER, IDR UNCHANGED		
		*	REGISTER - A,B,C,D,H,L ALTERED		
		*	COUNT - REGISTER B		
		*	Ø1=1 BYTE		
		*	ØØ=256 BYTES		
		*	ERROR - REGISTER A		
		*	Ø - NO ERRORS		
		*	1 - CRC ERROR		
		*	2 - BLOCK NOT FOUND		
		*	3 - END OF TAPE OR JAM		
		*	ENTRY POINTS:		
		*	READ - NORMAL ENTRY		
		*	ALTRD - DECK WILL BACKSPACE		
		*	FIRST, USER MUST SUPPLY RETRIES.		
		*	ALTRD2 - NORMAL, EXCEPT USER MUST		
		*	SUPPLY RETRIES.		
ØAB9	16ØA	READ	MVI	D,RETRYS	
ØABB	D5	RD54	PUSH	D	RETRYS, MODE
		ALTRD2	EQU	RD54	
ØABC	21ØØØØ	RD5	LXI	H,Ø	RESET CRC
ØABF	DBØ2		IN	TAPEIN	STATUS
ØAC1	57		MOV	D,A	
ØAC2	ØEEØ	RD51	MVI	C,EØH	READ
ØAC4	CD9BØA		CALL	CMDOUT	
ØAC7	7A		MOV	A,D	STOP?
ØAC8	E6Ø4		ANI	Ø4H	
ØACA	CAD7ØA		JZ	RD5Ø	NO
ØACD	3EØ4		MVI	A,4	.4 SECONDS
ØACF	CD81ØA		CALL	DELAY	
ØAD2	16ØØ		MVI	D,Ø	STATUS = Ø
ØAD4	C3C2ØA		JMP	RD51	
ØAD7	0630	RD50	MVI	B,30H	8 SECOND TIMEOUT
ØAD9	5Ø	RD57	MOV	D,B	
ØADA	DBØ2	RD53	IN	TAPEIN	STATUS

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
ØADC	E6ØF		ANI	ØFH	READY?
ØADE	C29ØØB		JNZ	RD1Ø	YES
ØAE1	1B		DCX	D	
ØAE2	14		INR	D	
ØAE3	15		DCR	D	
ØAE4	C2DAØA		JNZ	RD53	
ØAE7	Ø5		DCR	B	
ØAE8	C2D9ØA		JNZ	RD57	
ØAEB	CD4FØA		CALL	REWIND	
ØAEE	3EØ2	RD2	MVI	A,2	ERROR = 2
ØAFØ	D1		POP	D	RETRIES, MODE
ØAF1	15	RD8	DCR	D	
ØAF2	C2BBØA		JNZ	RD54	
ØAF5	C9		RET		
ØAF6	CD15ØA	RD52	CALL	GET	IDH
ØAF9	.41		MOV	B,C	
ØAFA	CD15ØA		CALL	GET	IDL
ØAFD	59		MOV	E,C	
ØAFE	CD15ØA		CALL	GET	COUNT
ØBØ1	51		MOV	D,C	
ØBØ2	CD15ØA		CALL	GET	CRC1
ØBØ5	CD15ØA		CALL	GET	CRC2
ØBØ8	97		SUB	A	CRC = Ø?
ØBØ9	84		ADD	H	
ØBØA	C2BCØA		JNZ	RD5	NO
ØBØD	85		ADD	L	
ØBØE	C2BCØA		JNZ	RD5	NO
		*	COMPUTE		BE TAPEID
		*			-HL IDR
		*			XY
ØB11	7B		MOV	A,E	
ØB12	2AB1ØA		LHLD	IDR	
ØB15	95		SUB	L	
ØB16	5F		MOV	E,A	REGISTER E CONTAINS Y
ØB17	6F		MOV	L,A	
ØB18	78		MOV	A,B	
ØB19	9C		SBB	H	REGISTER A CONTAINS X
ØB1A	67		MOV	H,A	H = XY/8
ØB1B	29		DAD	H	
ØB1C	29		DAD	H	
ØB1D	29		DAD	H	
ØB1E	29		DAD	H	
ØB1F	29		DAD	H	
ØB2Ø	7C		MOV	A,H	
ØB21	CA38ØB		JZ	ID1	
ØB24	F23DØB		JP	ID2	
ØB27	2F		CMA		COMPUTE FF DELAY
ØB28	C602		ADI	2	ADD 1+1 FOR 2'S COMP
ØB2A	FA32ØB		JM	ID3	
ØB2D	FEØ4		CPI	4	GREATER THAN THRESHOLD?

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
ØB2F	FABCØA		JM	RD5	NO
ØB32	CD7AØA	ID3	CALL	FF	
ØB35	C3BCØA		JMP	RD5	
ØB38	1C	ID1	INR	E	Y = Ø?
ØB39	1D		DCR	E	
ØB3A	CA45ØB		JZ	RD6	YES
ØB3D	C6Ø6	ID2	ADI	6	
ØB3F	CD68ØA		CALL	FR	
ØB42	C3EEØA		JMP	RD2	
ØB45	42	RD6	MOV	B,D	COUNT
ØB46	D1		POP	D	RETRIES, MODE
ØB47	C5		PUSH	B	COUNT
ØB48	2AB3ØA		LHLD	POINTR	
ØB4B	E5		PUSH	H	
ØB4C	21ØØØØ		LXI	H,Ø	RESET CRC
ØB4F	CD15ØA	RD56	CALL	GET	
ØB52	1C		INR	E	
ØB53	1D		DCR	E	
ØB54	C25BØB		JNZ	RD55	
ØB57	E3		XTHL		SWITCH CRC, POINTER
ØB58	71		MOV	M,C	STORE DATA
ØB59	23		INX	H	BUMP POINTER
ØB5A	E3		XTHL		SWITCH CRC, POINTER
ØB5B	Ø5	RD55	DCR	B	DECREMENT COUNT
ØB5C	C24FØB		JNZ	RD56	
ØB5F	C1		POP	B	ADJUST STACK POINTER
ØB6Ø	C1		POP	B	COUNT
ØB61	CD15ØA		CALL	GET	
ØB64	CD15ØA		CALL	GET	
ØB67	DBØ2		IN	TAPEIN	STATUS
ØB69	1F		RAR		OVERRUN?
ØB6A	DA7BØB		JC	ALTRD	YES
ØB6D	1F		RAR		
ØB6E	1F		RAR		STOP?
ØB6F	DA96ØB		JC	RD11	YES
ØB72	97		SUB	A	
ØB73	84		ADD	H	
ØB74	C27BØB		JNZ	ALTRD	NO
ØB77	85		ADD	L	
ØB78	CA85ØB		JZ	RD19	
ØB7B	3EØ5	ALTRD	MVI	A,5	GREATER THAN 1 BLOCK
ØB7D	CD68ØA		CALL	FR	
ØB8Ø	3EØ1		MVI	A,1	ERROR = 1
ØB82	C3F1ØA		JMP	RD8	
ØB85	5Ø	RD19	MOV	D,B	SAVE COUNT
ØB86	15		DCR	D	DECREMENT SAVED COUNT
ØB87	CD15ØA	RD9	CALL	GET	
ØB8A	14		INR	D	INCREMENT SAVED COUNT
ØB8B	C287ØB		JNZ	RD9	
ØB8E	97		SUB	A	ERROR = Ø

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
0B8F	C9		RET		
0B90	E604	RD10	ANI	04H	STOP?
0B92	CAF60A		JZ	RD52	NO
0B95	D1		POP	D	RETRIES, MODE
0B96	CD4F0A	RD11	CALL	REWIND	
0B99	3E03		MVI	A, 3	ERROR = 3
0B9B	C3F10A		JMP	RD8	
			END		

8080 DRIVER SOFTWARE (OCTAL)

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
		*		RECORD (UNTIL COUNT EXHAUSTED)	
		*		DECK IS STOPPED AFTER RETURN	
		*		INPUT:	
		*		DECK - DECK NUMBER LOCATED IN MEMORY	
		*		POINTW - LOCATED IN MEMORY	
		*		(FIRST DATA BYTE)	
		*		IDW - LOCATED IN MEMORY (FIRST BLOCK)	
		*		COUNT - REGISTER H,L	
		*		OUTPUT:	
		*		POINTW - LOCATED IN MEMORY	
		*		(LAST DATA BYTE + 1)	
		*		ERROR - REGISTER A	
		*		0 - NO ERRORS	
		*		1 - CRC ERROR IN BLOCK	
		*		IDW - 1	
		*		2 - BLOCK IDW-1 NOT FOUND	
		*		3 - TAPE END OR JAM	
		*		IDW - LOCATED IN MEMORY	
		*		(LAST BLOCK + 1)	
		*		ALTERED	
		*		REGISTERS - A,B,C,D,E,H,L, IDR, POINTR	
011	000	026 001	RECORD	MVI D,1	ERASE = 1
011	002	036 005		MVI E,5	STOPS = 5
011	004	345		PUSH H	COUNT
011	005	325	RCD20	PUSH D	ERASE, STOPS
011	006	052 265 012		LHLD IDW	
011	011	053		DCX H	IDR = IDW - 1
011	012	042 261 012		SHLD IDR	
011	015	043		INX H	
011	016	175		MOV A,L	IDW = 0 ?
011	017	264		ORA H	
011	020	312 051 011		JZ RCD10	YES
011	023	026 013		MVI D,11	RETRIES = 10
011	025	036 001		MVI E,1	CHECK MODE
011	027	315 173 013		CALL ALTRD	
011	032	074		INR A	ERROR?
011	033	075		DCR A	
011	034	312 066 011		JZ RCD13	NO
011	037	321	RCD12	POP D	ERASE, STOPS
011	040	341	RCD21	POP H	COUNT
011	041	016 220	RCD27	MVI C,90H	STOP
011	043	107		MOV B,A	SAVE ERROR
011	044	315 233 012		CALL CMDOUT	
011	047	170		MOV A,B	RESTORE ERROR
011	050	311		RET	
011	051	315 117 012	RCD10	CALL REWIND	
011	054	016 354		MVI C,ECH	ERASE

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
Ø11 Ø56	315 233 Ø12		CALL	CMDOUT	
Ø11 Ø61	Ø76 Ø5Ø		MVI	A, 4Ø	4 SECONDS
Ø11 Ø63	315 2Ø1 Ø12		CALL	DELAY	
Ø11 Ø66	321	RCD13	POP	D	ERASE, STOPS
Ø11 Ø67	325		PUSH	D	
Ø11 Ø7Ø	Ø25	RCD15	DCR	D	ERASE (ERASE-1) BLOCKS
Ø11 Ø71	312 111 Ø11		JZ	RCD14	
Ø11 Ø74	Ø16 354		MVI	C, ECH	ERASE
Ø11 Ø76	315 233 Ø12		CALL	CMDOUT	
Ø11 1Ø1	325		PUSH	D	
Ø11 1Ø2	315 332 Ø11		CALL	RECRD1	
Ø11 1Ø5	321		POP	D	
Ø11 1Ø6	3Ø3 Ø7Ø Ø11		JMP	RCD15	
Ø11 111	341	RCD14	POP	H	ERASE, STOPS
Ø11 112	321		POP	D	COUNT
Ø11 113	325		PUSH	D	
Ø11 114	345		PUSH	H	
Ø11 115	Ø52 267 Ø12		LHLD	POINTW	POINTER
Ø11 12Ø	Ø25	RCD19	DCR	D	COUNT HIGH = Ø?
Ø11 121	Ø24		INR	D	
Ø11 122	3Ø2 324 Ø11		JNZ	RCD16	NO
Ø11 125	Ø35		DCR	E	
Ø11 126	Ø34		INR	E	
Ø11 127	312 2Ø1 Ø11		JZ	RCD17	YES
Ø11 132	1Ø3		MOV	B, E	COUNT = COUNTL
Ø11 133	Ø36 ØØØ		MVI	E, Ø	COUNTL = Ø
Ø11 135	325	RCD18	PUSH	D	SAVE COUNT
Ø11 136	353		XCHG		
Ø11 137	Ø52 261 Ø12		LHLD	IDR	
Ø11 142	Ø43		INX	H	
Ø11 143	Ø42 261 Ø12		SHLD	IDR	
Ø11 146	353		XCHG		
Ø11 147	Ø16 35Ø		MVI	C, E8H	RECORD
Ø11 151	315 233 Ø12		CALL	CMDOUT	
Ø11 154	315 332 Ø11		CALL	RECRD1	
Ø11 157	333 ØØ2		IN	TAPEIN	ERROR?
Ø11 161	346 Ø15		ANI	ØDH	
Ø11 163	321		POP	D	GET COUNT
Ø11 164	312 12Ø Ø11		JZ	RCD19	NO
Ø11 167	321		POP	D	DCR STOPS
Ø11 17Ø	Ø35		DCR	E	Ø?
Ø11 171	3Ø2 ØØ5 Ø11		JNZ	RCD2Ø	NO
Ø11 174	Ø76 ØØ3		MVI	A, 3	ERROR = 3
Ø11 176	3Ø3 Ø4Ø Ø11		JMP	RCD21	
Ø11 2Ø1	Ø76 ØØ5	RCD17	MVI	A, 5	APPROXIMATELY 1Ø BLOCKS
Ø11 2Ø3	315 15Ø Ø12		CALL	FR	
Ø11 2Ø6	341		POP	H	ERASE, STOPS
Ø11 2Ø7	321		POP	D	COUNT
Ø11 21Ø	325	RCD26	PUSH	D	
Ø11 211	345		PUSH	H	
Ø11 212	227		SUB	A	COUNT = Ø?

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
Ø11 213	2Ø2		ADD	D	
Ø11 214	3Ø2 223 Ø11		JNZ	RCD22	NO
Ø11 217	2Ø3		ADD	E	
Ø11 22Ø	312 Ø37 Ø11		JZ	RCD12	YES
Ø11 223	Ø52 265 Ø12	RCD22	LHLD	IDW	
Ø11 226	Ø42 261 Ø12		SHLD	IDR	
Ø11 231	Ø26 ØØ6		MVI	D,6	RETRIES = 6
Ø11 233	Ø36 ØØ1		MVI	E,1	CHECK MODE
Ø11 235	315 273 Ø12		CALL	ALTRD2	
Ø11 24Ø	Ø74		INR	A	ERROR?
Ø11 241	Ø75		DCR	A	
Ø11 242	321		POP	D	
Ø11 243	312 252 Ø11		JZ	RCD24	NO
Ø11 246	Ø24		INR	D	INCREMENT ERASE
Ø11 247	3Ø3 ØØ5 Ø11		JMP	RCD2Ø	
Ø11 252	Ø26 ØØ1	RCD24	MVI	D,1	ERASE = 1
Ø11 254	Ø52 265 Ø12		LHLD	IDW	INCREMENT IDW
Ø11 257	Ø43		INX	H	
Ø11 26Ø	Ø42 265 Ø12		SHLD	IDW	
Ø11 263	353		XCHG		
Ø11 264	321		POP	D	
Ø11 265	Ø24		INR	D	COUNTH = Ø?
Ø11 266	Ø25		DCR	D	
Ø11 267	312 3Ø7 Ø11		JZ	RCD25	YES
Ø11 272	Ø25		DCR	D	DECREMENT COUNTH
Ø11 273	345		PUSH	H	
Ø11 274	Ø52 267 Ø12		LHLD	POINTW	
Ø11 277	Ø44		INR	H	
Ø11 3ØØ	Ø42 267 Ø12		SHLD	PQINTW	
Ø11 3Ø3	341		POP	H	
Ø11 3Ø4	3Ø3 21Ø Ø11		JMP	RCD26	
Ø11 3Ø7	Ø52 267 Ø12	RCD25	LHLD	POINTW	ADD COUNTL TO POINTER
Ø11 312	Ø26 ØØØ		MVI	D, Ø	
Ø11 314	Ø31		DAD	D	
Ø11 315	Ø42 267 Ø12		SHLD	POINTW	
Ø11 32Ø	227		SUB	A	ERROR = Ø
Ø11 321	3Ø3 Ø41 Ø11		JMP	RCD27	
Ø11 324	Ø25	RCD16	DCR	D	DECREMENT COUNTH
Ø11 325	ØØ6 ØØØ		MVI	B, Ø	COUNT = Ø
Ø11 327	3Ø3 135 Ø11		JMP	RCD18	

```

*
* RECRD1 (RECORD ONE BLOCK)
* RECORD OR ERASE COMMAND MUST BE ISSUED
* BEFORE CALLING.
* UNDERRUN AND STOP SHOULD BE CHECKED
* AFTER RETURN.
* INPUTS:
* DECK - DECK NUMBER LOCATED
* IN MEMORY
* ID - REGISTER D,E
* COUNT - REGISTER B
* (Ø1=1 BYTE, ØØ=256 BYTES)

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<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
		*		POINTER - REGISTER H,L	
		*		(FIRST DATA BYTE)	
		*		OUTPUT:	
		*		POINTER - REGISTER H,L	
		*		(LAST DATA BYTE + 1)	
		*		ALTERED	
		*		REGISTERS - A,B,C,D,E,H,L	
Ø11	332	345	RECRD1	PUSH H	PUSH POINTER
Ø11	333	Ø41 ØØØ ØØØ		LXI H,Ø	RESET CRC
Ø11	336	112		MOV C,D	ID HIGH
Ø11	337	315 111 Ø12		CALL ALTPUT	
Ø11	342	113		MOV C,E	ID LOW
Ø11	343	315 1Ø2 Ø12		CALL PUT	
Ø11	346	11Ø		MOV C,B	COUNT
Ø11	347	315 1Ø2 Ø12		CALL PUT	
Ø11	352	124		MOV D,H	SAVE CRC2
Ø11	353	115		MOV C,L	CRC1
Ø11	354	315 1Ø2 Ø12		CALL PUT	
Ø11	357	112		MOV C,D	CRC2
Ø11	36Ø	315 1Ø2 Ø12		CALL PUT	
Ø11	363	13Ø		MOV E,B	SAVE COUNT
Ø11	364	343	RECD1	XTHL	SWITCH CRC, POINTER
Ø11	365	116		MOV C,M	LOAD DATA
Ø11	366	Ø43		INX H	INCREMENT POINTER
Ø11	367	343		XTHL	SWITCH CRC, POINTER
Ø11	37Ø	315 1Ø2 Ø12		CALL PUT	
Ø11	373	ØØ5		DCR B	DECREMENT COUNT
Ø11	374	3Ø2 364 Ø11		JNZ RECD1	NOT ZERO
Ø11	377	124		MOV D,H	SAVE CRC2
Ø12	ØØØ	115		MOV C,L	CRC1
Ø12	ØØ1	315 1Ø2 Ø12		CALL PUT	
Ø12	ØØ4	112		MOV C,D	CRC2
Ø12	ØØ5	315 1Ø2 Ø12		CALL PUT	
Ø12	Ø1Ø	Ø35		DCR E	DECREMENT SAVED COUNT
Ø12	Ø11	315 1Ø2 Ø12	RECD3	CALL PUT	
Ø12	Ø14	Ø34		INR E	INCREMENT SAVED COUNT
Ø12	Ø15	3Ø2 Ø11 Ø12		JNZ RECD3	NOT ZERO
Ø12	Ø2Ø	315 1Ø2 Ø12		CALL PUT	
Ø12	Ø23	341		POP H	POP POINTER
Ø12	Ø24	311		RET	
		*		GET	
		*		CRC IN H,L	
		*		DATA RETURNED IN C	
		*		A,C,H,L, ALTERED	
Ø12	Ø25	333 ØØ2	GET	IN TAPEIN	STATUS
Ø12	Ø27	346 Ø17		ANI ØFH	
Ø12	Ø31	312 Ø25 Ø12		JZ GET	
Ø12	Ø34	315 217 Ø12		CALL DIN	
Ø12	Ø37	325	CRC	PUSH D	
Ø12	Ø4Ø	171		MOV A,C	
Ø12	Ø41	255		XRA L	

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
Ø12	Ø42		MOV	L,A	
Ø12	Ø43		MVI	E,7	ØØ7 TIMES
Ø12	Ø45		RAL		
Ø12	Ø46	CRCA	XRA	L	
Ø12	Ø47		DCR	E	
Ø12	Ø5Ø		JNZ	CRCA	DONE?
Ø12	Ø53		MOV	L,A	YES
Ø12	Ø54		RRC		
Ø12	Ø55		RRC		
Ø12	Ø56		MOV	E,A	SAVE 1
Ø12	Ø57		ANI	CØH	
Ø12	Ø61		XRA	H	
Ø12	Ø62		MOV	D,A	SAVE 2
Ø12	Ø63		MOV	A,E	RESTORE 1
Ø12	Ø64		ANI	3FH	
Ø12	Ø66		XRA	L	
Ø12	Ø67		MOV	H,A	CRC HIGH DONE
Ø12	Ø7Ø		RAL		TEST BIT 7
Ø12	Ø71		MOV	A,D	RESTORE 2
Ø12	Ø72		JNC	CRCFIN	BIT 7 WAS 1?
Ø12	Ø75		XRI	1	YES
Ø12	Ø77	CRCFIN	MOV	L,A	CRC LOW DONE
Ø12	1ØØ		POP	D	
Ø12	1Ø1		RET		
			PUT		
			DATA IN REGISTER C		
			CRC IN H,L		
			A,H,L ALTERED		
Ø12	1Ø2		PUT	IN TAPEIN	STATUS
Ø12	1Ø4		ANI	ØFH	
Ø12	1Ø6		JZ	PUT	
Ø12	111		ALTPUT	CALL DOUT	
Ø12	114		JMP	CRC	
			REWIND		
			REGISTER A, C ALTERED		
			THIS ROUTINE WILL GUARANTEE		
			DECK SELECTION		
Ø12	117		REWIND	MVI C,9ØH	STOP
Ø12	121		CALL	CMDOUT	
Ø12	124		REWB	IN TAPEIN	
Ø12	126		ANI	Ø8H	
Ø12	13Ø		JZ	REWB	
Ø12	133		MVI	C,8ØH	FR
Ø12	135		CALL	CMDOUT	
Ø12	14Ø		REWA	IN TAPEIN	
Ø12	142		ANI	8	
Ø12	144		JZ	REWA	
Ø12	147		RET		
			FAST REVERSE, FAST FORWARD		
			REGISTER A CONTAINS MULTIPLE		
			OF 1ØØ MILLI-SECONDS DELAY		
			REGISTER A ALTERED		

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
Ø12 15Ø	3Ø5	FR	PUSH	B	
Ø12 151	365		PUSH	PSW	
Ø12 152	Ø16 2ØØ		MVI	C, 8ØH	
Ø12 154	315 233 Ø12	FRA	CALL	CMDOUT	
Ø12 157	361		POP	PSW	
Ø12 16Ø	315 2Ø1 Ø12		CALL	DELAY	
Ø12 163	Ø16 22Ø		MVI	C, 9ØH	
Ø12 165	315 233 Ø12		CALL	CMDOUT	
Ø12 17Ø	3Ø1		POP	B	
Ø12 171	311		RET		
Ø12 172	3Ø5	FF	PUSH	B	
Ø12 173	365		PUSH	PSW	
Ø12 174	Ø16 24Ø		MVI	C, AØH	
Ø12 176	3Ø3 154 Ø12		JMP	FRA	
		::			DELAY MULTIPLE OF 1ØØ MS IN REGISTER A.
		::			REGISTERS A,B,C ALTERED
Ø12 2Ø1	ØØ1 ØØØ Ø4Ø	DELAY	LXI	B, 2ØØØH	
Ø12 2Ø4	Ø13	D1	DCX	B	
Ø12 2Ø5	ØØ4		INR	B	
Ø12 2Ø6	ØØ5		DCR	B	
Ø12 2Ø7	3Ø2 2Ø4 Ø12		JNZ	D1	
Ø12 212	Ø75		DCR	A	
Ø12 213	3Ø2 2Ø1 Ø12		JNZ	DELAY	
Ø12 216	311		RET		
		::			INPUT DATA BYTE (DATA RETURNED IN C)
		::			REGISTER A IS ALTERED
Ø12 217	Ø76 357	DIN	MVI	A, EFH	
Ø12 221	323 ØØ1		OUT	STROBE	
Ø12 223	333 ØØ2		IN	TAPEIN	
Ø12 225	117		MOV	C, A	
Ø12 226	Ø76 337	DINA	MVI	A, DFH	
Ø12 23Ø	323 ØØ1		OUT	STROBE	
Ø12 232	311		RET		
		::			OUTPUT COMMAND (DATA IN REGISTER C)
		::			DECK IS OR'D WITH DATA
		::			REGISTER A IS ALTERED
Ø12 233	Ø72 26Ø Ø12	CMDOUT	LDA	DECK	
Ø12 236	261		ORA	C	
Ø12 237	323 ØØ2		OUT	TAPOUT	
Ø12 241	Ø76 237		MVI	A, 9FH	
Ø12 243	323 ØØ1	CMDA	OUT	STROBE	
Ø12 245	3Ø3 226 Ø12		JMP	DINA	
		::			OUTPUT DATA (DATA IN REGISTER C)
		::			REGISTER A IS ALTERED
Ø12 25Ø	171	DOUT	MOV	A, C	
Ø12 251	323 ØØ2		OUT	TAPOUT	
Ø12 253	Ø76 137		MVI	A, 5FH	
Ø12 255	3Ø3 243 Ø12		JMP	CMDA	
		::			VARIABLE DATA AREA
Ø12 26Ø	ØØØ	DECK	DS	1	DECK NUMBER TO BE USED
Ø12 261	ØØØ ØØØ	IDR	DS	2	READ ID

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
Ø12 263	ØØØ ØØØ	POINTR	DS	2	READ POINTER
Ø12 265	ØØØ ØØØ	IDW	DS	2	WRITE ID
Ø12 267	ØØØ ØØØ	POINTW	DS	2	WRITE POINTER
		*		READ ONE BLOCK	
		*		DECK REMAINS RUNNING AFTER RETURN	
		*		INPUT:	
		*		DECK - DECK NUMBER LOCATED IN MEMORY	
		*		POINTR - LOCATED IN MEMORY	
		*		(FIRST BYTE)	
		*		IDR - LOCATED IN MEMORY	
		*		RETRYS - REGISTER D	
		*		(ALTRD ONLY)	
		*		MODE - REGISTER E	
		*		Ø=READ	
		*		1=CHECK	
		*		OUTPUT:	
		*		DECK, POINTER, IDR UNCHANGED	
		*		REGISTER - A,B,C,D,H,L ALTERED	
		*		COUNT - REGISTER B	
		*		Ø1=1 BYTE	
		*		ØØ=256 BYTES	
		*		ERROR - REGISTER A	
		*		Ø - NO ERRORS	
		*		1 - CRC ERROR	
		*		2 - BLOCK NOT FOUND	
		*		3 - END OF TAPE OR JAM	
		*		ENTRY POINTS:	
		*		READ - NORMAL ENTRY	
		*		ALTRD - DECK WILL BACKSPACE	
		*		FIRST, USER MUST SUPPLY RETRIES.	
		*		ALTRD2 - NORMAL, EXCEPT USER MUST	
		*		SUPPLY RETRIES	
Ø12 271	Ø26 Ø12	READ	MVI	D, RETRYS	
Ø12 273	325	RD54	PUSH	D	RETRYS, MODE
		ALTRD2	EQU	RD54	
Ø12 274	Ø41 ØØØ ØØØ	RD5	LXI	H, Ø	RESET CRC
Ø12 277	333 ØØ2		IN	TAPEIN	STATUS
Ø12 3Ø1	127		MOV	D, A	
Ø12 3Ø2	Ø16 34Ø	RD51	MVI	C, EØH	READ
Ø12 3Ø4	315 233 Ø12		CALL	CMDOUT	
Ø12 3Ø7	172		MOV	A, D	STOP?
Ø12 31Ø	346 ØØ4		ANI	Ø4H	
Ø12 312	312 327 Ø12		JZ	RD5Ø	NO
Ø12 315	Ø76 ØØ4		MVI	A, 4	.4 SECONDS
Ø12 317	315 2Ø1 Ø12		CALL	DELAY	
Ø12 322	Ø26 ØØØ		MVI	D, Ø	STATUS = Ø
Ø12 324	3Ø3 3Ø2 Ø12		JMP	RD51	
Ø12 327	ØØ6 Ø6Ø	RD5Ø	MVI	B, 3ØH	8 SECOND TIMEOUT
Ø12 331	12Ø	RD57	MOV	D, B	
Ø12 332	333 ØØ2	RD53	IN	TAPEIN	STATUS

<u>_OC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENTS</u>
Ø12 334	346 Ø17		ANI	ØFH	READY?
Ø12 336	3Ø2 22Ø Ø13		JNZ	RD1Ø	YES
Ø12 341	Ø33		DCX	D	
Ø12 342	Ø24		INR	D	
Ø12 343	Ø25		DCR	D	
Ø12 344	3Ø2 332 Ø12		JNZ	RD53	
Ø12 347	ØØ5		DCR	B	
Ø12 35Ø	3Ø2 331 Ø12		JNZ	RD57	
Ø12 353	315 117 Ø12		CALL	REWIND	
Ø12 356	Ø76 ØØ2	RD2	MVI	A, 2	ERROR = 2
Ø12 36Ø	321		POP	D	RETRIES, MODE
Ø12 361	Ø25	RD8	DCR	D	
Ø12 362	3Ø2 273 Ø12		JNZ	RD54	
Ø12 365	311		RET		
Ø12 366	315 Ø25 Ø12	RD52	CALL	GET	IDH
Ø12 371	1Ø1		MOV	B, C	
Ø12 372	315 Ø25 Ø12		CALL	GET	IDL
Ø12 375	131		MOV	E, C	
Ø12 376	315 Ø25 Ø12		CALL	GET	COUNT
Ø13 ØØ1	121		MOV	D, C	
Ø13 ØØ2	315 Ø25 Ø12		CALL	GET	CRC1
Ø13 ØØ5	315 Ø25 Ø12		CALL	GET	CRC2
Ø13 Ø1Ø	227		SUB	A	CRC = Ø?
Ø13 Ø11	2Ø4		ADD	H	
Ø13 Ø12	3Ø2 274 Ø12		JNZ	RD5	NO
Ø13 Ø15	2Ø5		ADD	L	
Ø13 Ø16	3Ø2 274 Ø12		JNZ	RD5	NO
		**	COMPUTE		BE TAPEID
		**			-HL IDR
		**			XY
Ø13 Ø21	173		MOV	A, E	
Ø13 Ø22	Ø52 261 Ø12		LHLD	IDR	
Ø13 Ø25	225		SUB	L	
Ø13 Ø26	137		MOV	E, A	REGISTER E CONTAINS Y
Ø13 Ø27	157		MOV	L, A	
Ø13 Ø3Ø	17Ø		MOV	A, B	
Ø13 Ø31	234		SBB	H	REGISTER A CONTAINS X
Ø13 Ø32	147		MOV	H, A	H = XY/8
Ø13 Ø33	Ø51		DAD	H	
Ø13 Ø34	Ø51		DAD	H	
Ø13 Ø35	Ø51		DAD	H	
Ø13 Ø36	Ø51		DAD	H	
Ø13 Ø37	Ø51		DAD	H	
Ø13 Ø4Ø	174		MOV	A, H	
Ø13 Ø41	312 Ø7Ø Ø13		JZ	ID1	
Ø13 Ø44	362 Ø7Ø Ø13		JP	ID2	
Ø13 Ø47	Ø57		CMA		COMPUTE FF DELAY
Ø13 Ø5Ø	3Ø6 ØØ2		ADI	2	ADD 1+1 FOR 2'S COMP
Ø13 Ø52	372 Ø62 Ø13		JM	ID3	
Ø13 Ø55	376 ØØ4		CPI	4	GREATER THAN THRESHOLD?

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>	
Ø13	Ø57	372 274 Ø12	JM	RD5	NO	
Ø13	Ø62	315 172 Ø12	CALL	FF		
Ø13	Ø65	3Ø3 274 Ø12	JMP	RD5		
Ø13	Ø7Ø	Ø34	ID1	INR	E	Y = Ø?
Ø13	Ø71	Ø35		DCR	E	
Ø13	Ø72	312 1Ø5 Ø13	JZ	RD6	YES	
Ø13	Ø75	3Ø6 ØØ6	ID2	ADI	6	
Ø13	Ø77	315 15Ø Ø12	CALL	FR		
Ø13	1Ø2	3Ø3 356 Ø12	JMP	RD2		
Ø13	1Ø5	1Ø2	RD6	MOV	B, D	COUNT
Ø13	1Ø6	321		POP	D	RETRIES, MODE
Ø13	1Ø7	3Ø5		PUSH	B	COUNT
Ø13	11Ø	Ø52 263 Ø12	LHLD	POINTR		
Ø13	113	345		PUSH	H	
Ø13	114	Ø41 ØØØ ØØØ	LXI	H, Ø	RESET CRC	
Ø13	117	315 Ø25 Ø12	RD56	CALL	GET	
Ø13	122	Ø34		INR	E	
Ø13	123	Ø35		DCR	E	
Ø13	124	3Ø2 133 Ø13	JNZ	RD55		
Ø13	127	343		XTHL		SWITCH CRC, POINTER
Ø13	13Ø	161		MOV	M, C	STORE DATA
Ø13	131	Ø43		INX	H	BUMP POINTER
Ø13	132	343		XTHL		SWITCH CRC, POINTER
Ø13	133	ØØ5	RD55	DCR	B	DECREMENT COUNT
Ø13	134	3Ø2 117 Ø13	JNZ	RD56		
Ø13	137	3Ø1		POP	B	ADJUST STACK POINTER
Ø13	14Ø	3Ø1		POP	B	COUNT
Ø13	141	315 Ø25 Ø12	CALL	GET		
Ø13	144	315 Ø25 Ø12	CALL	GET		
Ø13	147	333 ØØ2	IN	TAPEIN	STATUS	
Ø13	151	Ø37	RAR		OVERRUN?	
Ø13	152	332 173 Ø13	JC	ALTRD	YES	
Ø13	155	Ø37	RAR			
Ø13	156	Ø37	RAR		STOP?	
Ø13	157	332 226 Ø13	JC	RD11	YES	
Ø13	162	227		SUB	A	
Ø13	163	2Ø4		ADD	H	
Ø13	164	3Ø2 173 Ø13	JNZ	ALTRD	NO	
Ø13	167	2Ø5		ADD	L	
Ø13	17Ø	312 2Ø5 Ø13	JZ	RD19		
Ø13	173	Ø76 ØØ5	ALTRD	MVI	A, 5	GREATER THAN 1 BLOCK
Ø13	175	315 15Ø Ø12	CALL	FR		
Ø13	2ØØ	Ø76 ØØ1	MVI	A, 1	ERROR = 1	
Ø13	2Ø2	3Ø3 361 Ø12	JMP	RD8		
Ø13	2Ø5	12Ø	RD19	MOV	D, B	SAVE COUNT
Ø13	2Ø6	Ø25		DCR	D	DECREMENT SAVED COUNT
Ø13	2Ø7	315 Ø25 Ø12	RD9	CALL	GET	
Ø13	212	Ø24		INR	D	INCREMENT SAVED COUNT
Ø13	213	3Ø2 2Ø7 Ø13	JNZ	RD9		
Ø13	216	227		SUB	A	ERROR = Ø

<u>LOC</u>	<u>OBJ</u>	<u>LABEL</u>	<u>OP</u>	<u>OPERAND</u>	<u>COMMENT</u>
Ø13 217	311		RET		
Ø13 22Ø	346 ØØ4	RD1Ø	ANI	Ø4H	STOP?
Ø13 222	312 366 Ø12		JZ	RD52	NO
Ø13 225	321		POP	D	RETRIES, MODE
Ø13 226	315 117 Ø12	RD11	CALL	REWIND	
Ø13 231	Ø76 ØØ3		MVI	A, 3	ERROR = 3
Ø13 233	3Ø3 361 Ø12		JMP	RD8	

K. PHI-DECK MAINTENANCE

Recommended Field Maintenance

This maintenance schedule consists of recommended maintenance operations to be performed in the field by operating personnel and service technicians. Schedule A consists of cleaning operations that should be performed every ten to twenty hours of operating time. Since the accumulation of dirt and tape oxide is highly dependent upon operating environment and the quality of tape used, the time interval for Schedule A can be varied according to system experience. The Schedule A cleaning operations are simple enough that they can be performed by operating personnel in many systems.

The items in Schedule B should be performed by technically skilled personnel.

Required Equipment

For Schedule A

1. Tape head cleaner or pure isopropyl alcohol
2. Rubber drive cleaner
3. Cotton tip wood swabs (Q-Tips)
4. Soft bristled brush
5. Tape head demagnetizer

Additional Equipment for Schedule B

1. Lightweight machine oil
2. SAE 10 wt. oil
3. Speed test tape
4. Oscilloscope, frequency counter or wow and flutter meter with speed check capability

Schedule A (10 to 20 hour intervals)

1. Remove accumulated dust, tape oxide particles, etc. with a soft bristled brush.
2. Clean magnetic head and tape guides with tape head cleaner or isopropyl alcohol.
3. Clean the capstan shaft with a cotton tip swab moistened with tape head cleaner. Do not allow tape head cleaner to run down the capstan shaft into the capstan bearing. Use only enough cleaning liquid on the cotton tip swab to remove tape oxide from the exposed portion of the capstan shaft.
4. Clean pinch roller with rubber drive cleaner or isopropyl alcohol.
5. Demagnetize the tape head using a tape head demagnetizer.

Schedule B (500 hour intervals)

1. Perform Schedule A.
2. Oil the capstan bearing using a drop of lightweight machine oil. Clean excess oil off the capstan shaft.
3. Oil the headbar pivot bushings with a drop or two of SAE 10 weight oil.
4. Check and adjust tape speed as described in the Motor Speed Calibration paragraph in section VI.

Maintenance Guide

This maintenance schedule consists of recommended maintenance checks and operations to be performed in a facility equipped for tape deck repairs and maintenance. For greatest system reliability, this procedure should be performed on a regular basis at intervals of approximately 1,000 hours of tape deck operating time. Where such maintenance is not performed on a scheduled basis, this routine should be performed whenever a tape deck is returned to a repair facility for repairs.

Required Equipment

1. Tape head cleaner or pure isopropyl alcohol
2. Rubber drive cleaner
3. Lightweight machine oil
4. SAE 10 wt. oil
5. Cotton tip wood swabs (Q-Tips)
6. Soft bristled brush
7. Tape head demagnetizer
8. Information Terminals M-300 Tape head and guide gauge set
9. Oscilloscope
10. Test tapes
11. Miscellaneous hand tools
12. Frequency counter

Cleaning

1. Clean Phi-Deck thoroughly. Remove accumulated dust, tape oxide particles and lint with air hose or brush.
2. Demagnetize tape head.
3. Clean tape head and tape guides with liquid cleaner and cotton swab. Use only a commercial tape head cleaning fluid or pure isopropyl alcohol.
4. Clean capstan shaft with a cotton tip wood swab moistened with tape head cleaner. Do not allow tape head cleaner to run down the capstan shaft into the capstan bearing. Use only enough cleaning liquid on the cotton swab to remove tape oxide from the exposed portion of the capstan shaft.
5. Clean capstan drive rubber roller. Use rubber drive roller cleaner or pure isopropyl alcohol.

Lubrication

1. Oil the headbar pivot bushings using a drop or two of SAE 10 weight oil. Wipe off excess oil.
2. Apply a drop of lightweight machine oil to the capstan bearing where the capstan shaft enters the bearing. Clean any excess oil from the capstan shaft.

Drive Belts

1. Remove the plastic cassette well and check the two reel drive belts. The belts should be replaced if there are any signs of splitting, cracking, or wear.
2. Check the belts for slippage by stalling the associated reel post while in the Fast Forward mode for the takeup reel and Rewind mode for the rewind reel. The belts should be replaced and the pulleys cleaned if there is belt slippage during the stalled condition.
3. Check the capstan flywheel drive belt for cracking, splitting, or wear. Replace if necessary.

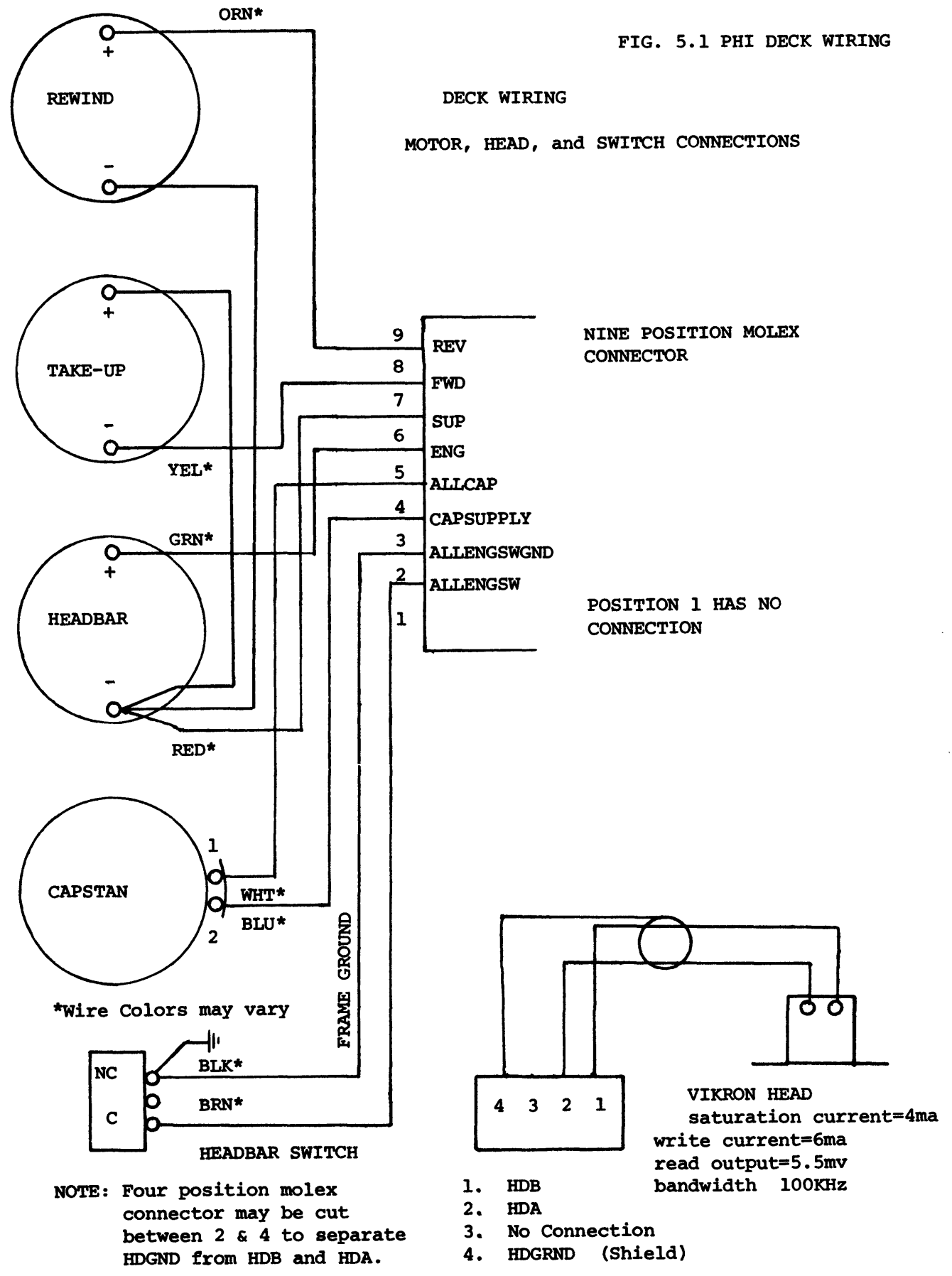
Alignment Checks and Adjustments

1. Using the Information Terminals M-300 gauge set and with the headbar engaged, check head depth of penetration, zenith and guide height. The parameters being out of tolerance indicate that the gearbox positioning may need to be adjusted to compensate for starwheel assembly wear.
2. If the previous checks indicate head misalignment due to gearbox positioning, perform gearbox assembly alignment procedure. If head alignment is correct, do not perform adjustment.
3. Check gearbox starwheel to headbar engage-disengage positioning. Adjust starwheel position sensing micro-switch for correct positioning if necessary.
4. Check pinch roller pressure and adjust if necessary.
5. Using a high quality tape with a continuously recorded tone or flux reversal pattern, check the play or read head output for signal levels and quality. Incorrect signals are indicative of head wear, head alignment or tape tracking problems.
6. Check tape speed and adjust as described in the Motor Speed Calibration paragraph in section VI.

298-051 PHI-F DOC

FIG. 5.1 PHI DECK WIRING

DECK WIRING
MOTOR, HEAD, and SWITCH CONNECTIONS



NOTE: Four position molex connector may be cut between 2 & 4 to separate HDGND from HDB and HDA.

- 1. HDB
- 2. HDA
- 3. No Connection
- 4. HDGRND (Shield)

The Digital Group Cassette Storage System

System Improvements

The following suggestions consist of various hardware and software improvements that may be made to the Cassette Storage System. Each modification should be examined to verify that it has not already been implemented.

NOTE: The hardware modifications are applicable only to The Digital Group B and C version controller cards. This board is identified by part number DG-0006-B or DG-0006-C on the right edge of the card. It is suggested that owners of A-version cards (DG-0006-A) purchase the controller upgrade kit. Refer to the schematic and parts placement diagram of the Cassette Storage System when making the hardware modifications.

Problems and associated modifications:

- I. A. Symptom: The Phideck head may attempt to engage when power is initially applied to the system.
- B. Modification (applicable only for B-version cards):
 1. Replace R42 with a 22K ohm resistor.
 2. Install a 4.7mfd, or greater tantalum capacitor from pin B (MANSTOP) on the dual 36-pin edge to GND.
- II. A. Symptom: The head will not engage properly or at all if a slow forward command is issued while the tape is moving in a fast forward mode.
- B. Modification (applicable only for B-version cards): See Fig. 1
 1. Cut the printed circuit trace leading to pin 4 of IC17 on the component side of the card.
 2. Solder a short piece of wire between pin 4 and 5 of IC17 on the circuit side of the card.

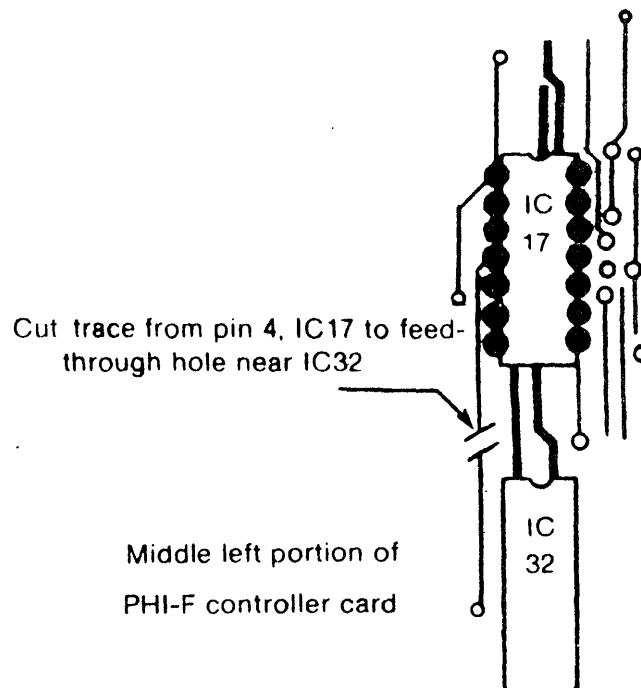


FIGURE 1

- III. A. Symptom: Abnormally high soft error rate with some types of tapes or cassettes.
NOTE: This modification will reduce the speed tolerance from 20% to approximately 15%, which should be sufficient for most applications.
- B. Modification:
 1. Replace R50 with a 33K ohm resistor.
 2. Replace C27 with a 4.7mfd tantalum capacitor.
- IV. A. Symptom: Several problems have arisen with the use of some cassette tapes, such as: long leaders, C60 or longer tapes with abnormally low drag, and tape jumping off the internal guides of the cassette, thus creasing the tape.
- B. Modification: Figures 1 and 2 contain software modifications that should be made to the system. There are two listings, one for the driver routines located at octal 011000 and another for the same driver routines located at octal 344000 in PHIMON. These changes will cure the above symptom and also provide a slight improvement in the access time of the Cassette Storage System.
- C. Procedure for modifying PHIMON:
 1. Power on system.
 2. Type DTO, then hit RETURN.
 3. Make the modifications shown in Figure 1 to the driver routines using DTO.
 4. Return to PHIMON using the reset button.
 5. Place a blank tape in drive #1.
 6. Type ZE!#1, then hit RETURN.
 7. Type BU#1, then hit RETURN.
 8. When the operation is finished, drive #1 will contain a system tape with the modifications.
 9. This new tape may now be used as your new system tape for all future operations.

WARNING: Do not use the modified version of PHIMON to save data or tapes with unmodified PHIMON or the directory will be lost. It is recommended that new tapes be generated using the modified PHIMON, and PIP be used transfer the data on the old tapes to the new ones.

- V. A. Symptom: The head on a Phideck may bang in and out when power is turned on or after a static discharge to the system cabinet or electronics.
- B. Solution:
 1. Immediately turn off power to the system.
 2. Move the system to an area that does not have a carpet or other static-producing media.
 3. Inspect all drives to be sure all the heads are disengaged. If one is engaged, turn the engage cam on the left side of the drive *counter clockwise* until the head is disengaged.
- VI. A. Symptom: Excessive errors on tapes due to contamination resulting from removing tapes from the drives without the tapes being rewound.
- B. Solution: Rewind all tapes before removing them from the drives. The following HOME command should be added to the PHIMON operating system tape to aid the user in rewinding tapes.
- C. HOME Command
 1. Usage

The HOme command allows the user to quickly rewind any Phideck drive. The command is executed by typing:

<HO#N or
<HOME#N

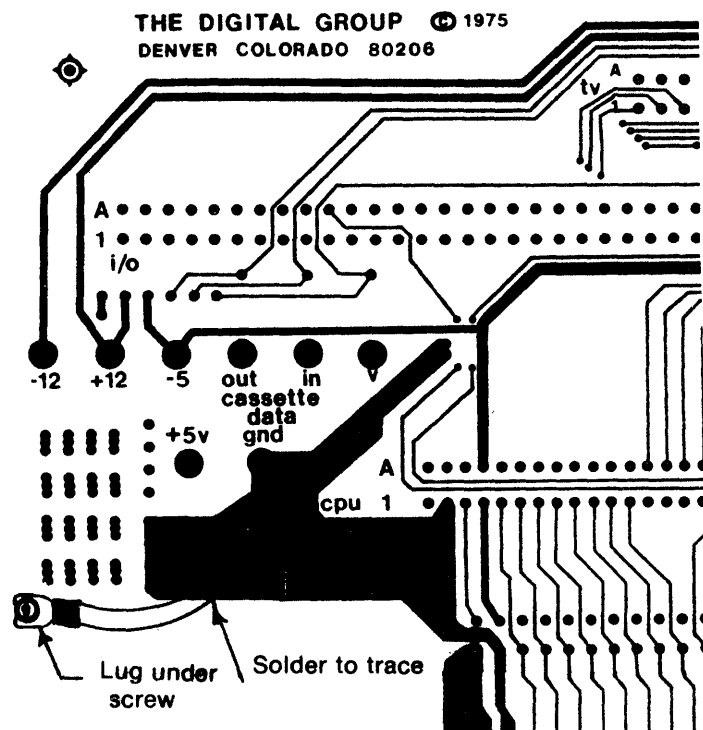
The "<" indicates the prompt on the monitor. N is the drive number (0-3). Drive number 0 will be rewound if N is not specified.
 2. Inserting the HOME Routine
 - a. Load PHIMON as usual.
 - b. Type AL #10, then hit RETURN.
 - c. Type DTO, then hit RETURN.
 - d. Type 010207 Octal.
 - e. Using DTO and referring to Figure 2, type Overlay 10 into memory.
 - f. Press the (ESC) key.
 - g. Type IN#10, then hit RETURN.
 - h. Type DTO, then hit RETURN.

- i. Using DTO and referring to Figure 3, type in the changes to the command table and the Home Routine.
- j. Press the (ESC) Key.
- k. Type BUILD, then hit RETURN.
- l. Modifications to PHIMON are now complete.

- VII. A. Symptom: Poor performance due to type of tape being used.
- B. Solution: Use only types of tape recommended by the Digital Group.
1. Digital Group audio cassettes are available in quantities of 1, 5 or 10 cassettes. Order number Cassette10 for 10 tapes, Cassette5 for 5 tapes.
 2. Use only high quality, low noise audio cassettes. Avoid high-output, chromium dioxide or any other special purpose tapes.
- VIII. A. Symptom: Excessive noise caused by a ground loop in system ground, resulting in excessive soft errors during read.
- B. Solution: Modify your system by grounding the system motherboard to the chassis. For a Digital Group system, this is best accomplished by soldering a short piece of 14 gauge wire to the ground plane on the top side of the motherboard and connecting the other end under a motherboard mounting screw with a lug affixed to the wire.

See the accompanying figure below.

NOTE: If, after accomplishing all the modifications and following all our suggestions, you are still unable to get satisfactory operation of your Phideck system, send your Phideck components or, for best results, your complete system, to us for repair and/or evaluation. It will be returned to you operational and with an extended 90-day warranty. Consult the Digital Group repair fee schedule for the cost of this service.



PATCH SHEET FOR PHIMON

Figure 1 — Modifications to PHIMON

ADDRESS	OBJECT CODE			
064265		0100	ORG EQU	344000
344062		0110	ST	ORG+62
344062		0120	**** FIVE SECOND DELAY FOR BLOCK 0. ****	
344062		0130	DB	062
062				
344202		0140	ST	ORG+202
344202		0150	**** BACKSPACE SEVERAL BLOCKS BEFORE CHECK READ	
344202		0160	DB	003
003				
345165		0170	ST	ORG+1165
345165		0180	**** JUMP TO STOP. ****	
345165	303 302 345	0190	JP	STOP
345277		0200	ST	ORG+1277
345277		0210	**** STOP ROUTINE AND FAST REVERSE CORRECTION.	
345277	303 322 345	0220	JP	RD51
345302	315 233 345	0230	STOP	CALL CMDOUT STOP ROUTINE
345305	076 001	0240	LD	A,1 .1 SECOND
345307	315 201 345	0250	CALL	DELAY
345312	301	0260	POP	BC
345313	311	0270	RET	
345314	315 150 345	0280	FRCOR	CALL FR FAST REVERSE CORRECTION
345317	303 356 345	0290	JP	RD2
345322	016 340	0300	RD51	LD C,0E0H READ
345324	315 233 345	0310	CALL	CMDOUT
345327	006 110	0320	RD50	LD B,110 14 SECONDS
346036		0330	ST	ORG+2036
346036		0340	**** SEARCH IMPROVEMENT. ****	
346036	174	0350	LD	A,H
346037	051	0360	ADD	HL,HL
346040	312 070 346	0370	JP	Z,ID1
346043	362 075 346	0380	JP	P,ID2
346046	204	0390	ADD	H
346051		0400	ST	ORG+2051
346051		0410	**** MORE SEARCH IMPROVEMENT. ****	
346051		0420	DB	1
001				
346056		0430	ST	ORG+2056
346056		0440	**** MORE SEARCH IMPROVEMENT. ****	
346056		0450	DB	3
003				
346075		0460	ST	ORG+2075
346075		0470	**** MORE SEARCH IMPROVEMENT. ****	
346075	204	0480	IL2	ADD H
346076	007	0490	RLCA	
346077	306 005	0500	ADD	5
346101	303 314 345	0510	JP	FRCOR
346174		0520	ST	ORG+2174
346174		0530	**** LAST OF SEARCH IMPROVEMENT. ****	
346174		0540	DB	3
003				
346175		0550	**** EXTERNAL REFERENCES. ****	
346175		0560	CMDOUT	EQU ORG+1233
346175		0570	DELAY	EQU ORG+1201
346175		0580	FR	EQU ORG+1150
346175		0590	ID1	EQU ORG+2070
346175		0600	RD2	EQU ORG+1356
346175		0610	END	

PATCH SHEET FOR PHIDECK DRIVER

Figure 2 — Modifications to the Phi-Deck Driver Routines

ADDRESS	OBJECT CODE	0100	ORG	EQU	011000
064240		0110		ST	ORG+62
011062		0120	****	FIVE SECOND DELAY FOR FLOCK 0. ****	
011062		0130		DB	062
062					
011202		0140		ST	ORG+202
011202		0150	****	BACKSPACE SEVERAL FLOCKS BEFORE CHECK READ.	
011202		0160		DB	003
003					
012165		0170		ST	ORG+1165
012165		0180	****	JUMP TO STOP. ****	
012165	303 302 012	0190		JP	STOP
012277		0200		ST	ORG+1277
012277		0210	****	STOP ROUTINE AND FAST REVERSE CORRECTION.	
012277	303 322 012	0220		JP	RD51
012302	315 233 012	0230	STOP	CALL CMDOUT STOP ROUTINE	
012305	076 001	0240		LD	A,1 .1 SECOND
012307	315 201 012	0250		CALL	DELAY
012312	301	0260		POP	BC
012313	311	0270		RET	
012314	315 150 012	0280	FRCOR	CALL FR FAST REVERSE CORRECTION	
012317	303 356 012	0290		JP	RD2
012322	016 340	0300	RD51	LD	C,0E0H READ
012324	315 233 012	0310		CALL	CMDOUT
012327	006 110	0320	RD50	LD	B,110 14 SECONDS
013036		0330		ST	ORG+2036
013036		0340	****	SEARCH IMPROVEMENT. ****	
013036	174	0350		LD	A,H
013037	051	0360		ADD	HL,HL
013040	312 070 013	0370		JP	Z,ID1
013043	362 075 013	0380		JP	P,ID2
013046	204	0390		ADD	H
013051		0400		ST	ORG+2051
013051		0410	****	MORE SEARCH IMPROVEMENT. ****	
013051		0420		DB	1
001					
013056		0430		ST	ORG+2056
013056		0440	****	MORE SEARCH IMPROVEMENT. ****	
013056		0450		DB	3
003					
013075		0460		ST	ORG+2075
013075		0470	****	MORE SEARCH IMPROVEMENT. ****	
013075	204	0480	ID2	ADD	H
013076	007	0490		RLCA	
013077	300 005	0500		ADD	5
013101	303 314 012	0510		JP	FRCOR
013174		0520		ST	ORG+2174
013174		0530	****	LAST OF SEARCH IMPROVEMENT. ****	
013174		0540		DB	3
003					
013175		0550	****	EXTERNAL REFERENCES. ****	
013175		0560	CMDOUT	EQU	ORG+1233
013175		0570	DELAY	EQU	ORG+1201
013175		0580	FR	EQU	ORG+1150
013175		0590	ID1	EQU	ORG+2070
013175		0600	RD2	EQU	ORG+1356
013175		0610		END	

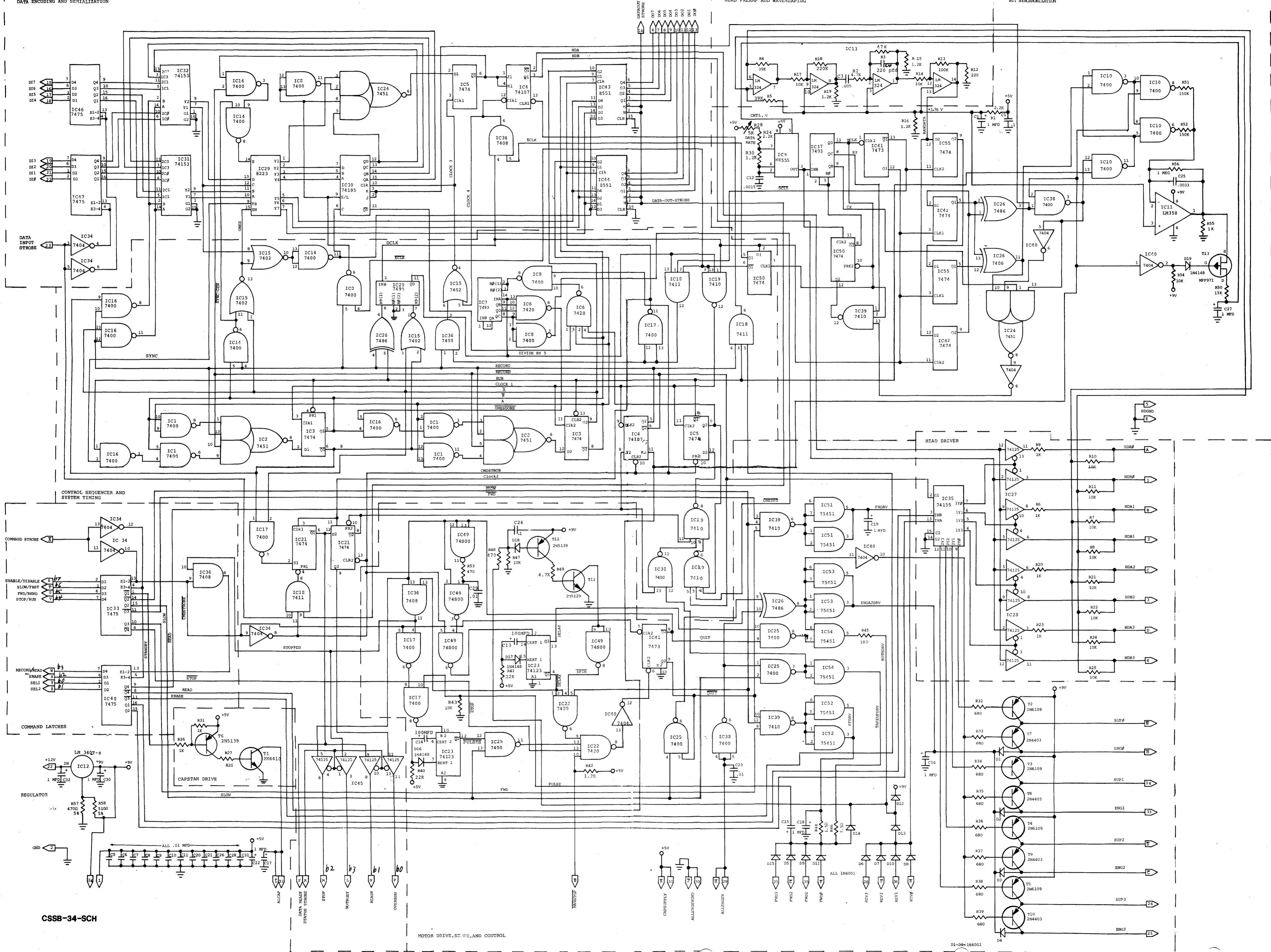
PHIMON HOME COMMAND

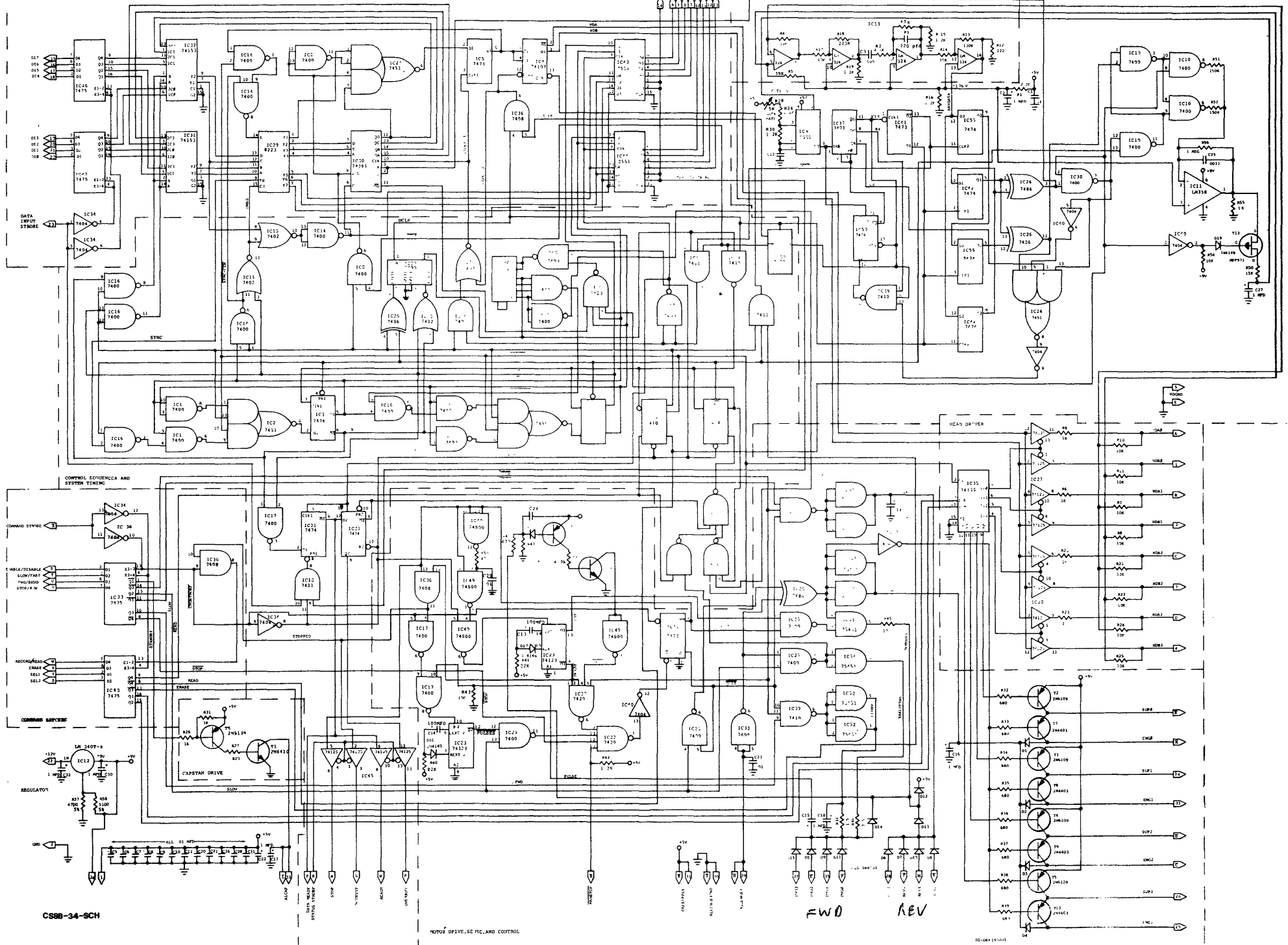
LOCATION				
010207	OBJECT CODE	0100	ST	010207
010207		0110	* PATCHES TO OVERLAY 10 FOR HOME COMMAND	
010207	310 317	0120	DC	'HO'
010211	355 345	0130	DW	345355
010213	016	0140	DB	016
010214	332 305	0150	DC	'ZE'
010216	362 357	0160	DW	357362
010220	012	0170	DB	012
010221	311 316	0180	DC	'IN'
010223	363 345	0190	DW	345363
010225	362 364	0210	DW	364362
010227	065	0220	DB	065
010230	000	0230	DB	000

FIGURE 3 -- Patches to Help Overlay

LOCATION				
340146	OBJECT CODE	0240	ST	340146
340146		0250	* MODIFICATION TO PHIMON TO ADD 'HOME'	
340146		0260	* COMMAND, WHICH WILL REWIND THE SPECIFIED	
340146		0270	* PHIDECK DRIVE UNIT. BY TOM COX	
340146		0280	*	
340146		0290	* FORMAT >HOME#N	
340146		0300	*	
340146		0310	* NEW ENTRY FOR COMMAND TABLE	
340146	020	0320	COMTAB DB	020
340262		0330	ST	340262
340262	310 317	0340	DC	'HO'
340264	352 343	0350	DW	HOME
340266	000	0360	DB	0
343352		0370	ST	343352
343352		0380	* ROUTINE TO REWIND SPECIFIED DECK	
343352	315 162 341	0390	HOME CALL DECKSL	
343355	315 117 345	0400	CALL REWIND	
343360	303 042 340	0410	JP COMAND	
343363		0420	DECKSL EQU 341162	
343363		0430	REWIND EQU 345117	
343363		0440	COMAND EQU 340042	

FIGURE 4 -- Patches to Command Table





TWO AND FOUR DRIVE CABINET ASSEMBLY INSTRUCTIONS

CASSETTE STORAGE CABINET PARTS LIST

NOTE: Parts are subject to change without notice due to supplier availability.

1	Upper Cover	Small parts bag (all cabinets):
1	Lower Cover	2 4-40x1/2" screws
2	Side Rails	2 4-40 nuts
1	Front Dress Panel	12 8-32x1/4" screws
1	Front Panel	2 8-32x1/2" screws
1	Rear Panel	18 6-32x1/2" screws
4	Rubber Furniture Guards	18 6-32 nuts
		1 36 pin connector

TWO AND FOUR DRIVE CABINET ASSEMBLY INSTRUCTIONS

A. LOWER COVER

1. Locate the 4 holes nearest the corners. These will be used to mount the rubber feet. In addition, the 2 holes near the front lip will also be used to mount two of the drives. To mount a rubber foot, insert one 6-32x1/2" screw into the foot, then through the bottom of the lower cover.

NOTE: The two screws used to mount the front feet are also used to help mount two of the drives and extend up into the cabinet.

2. Position the drives over the remaining holes, then install the 6-32x1/2" screws through the drive legs and through the bottom cover. Do not tighten at this point.

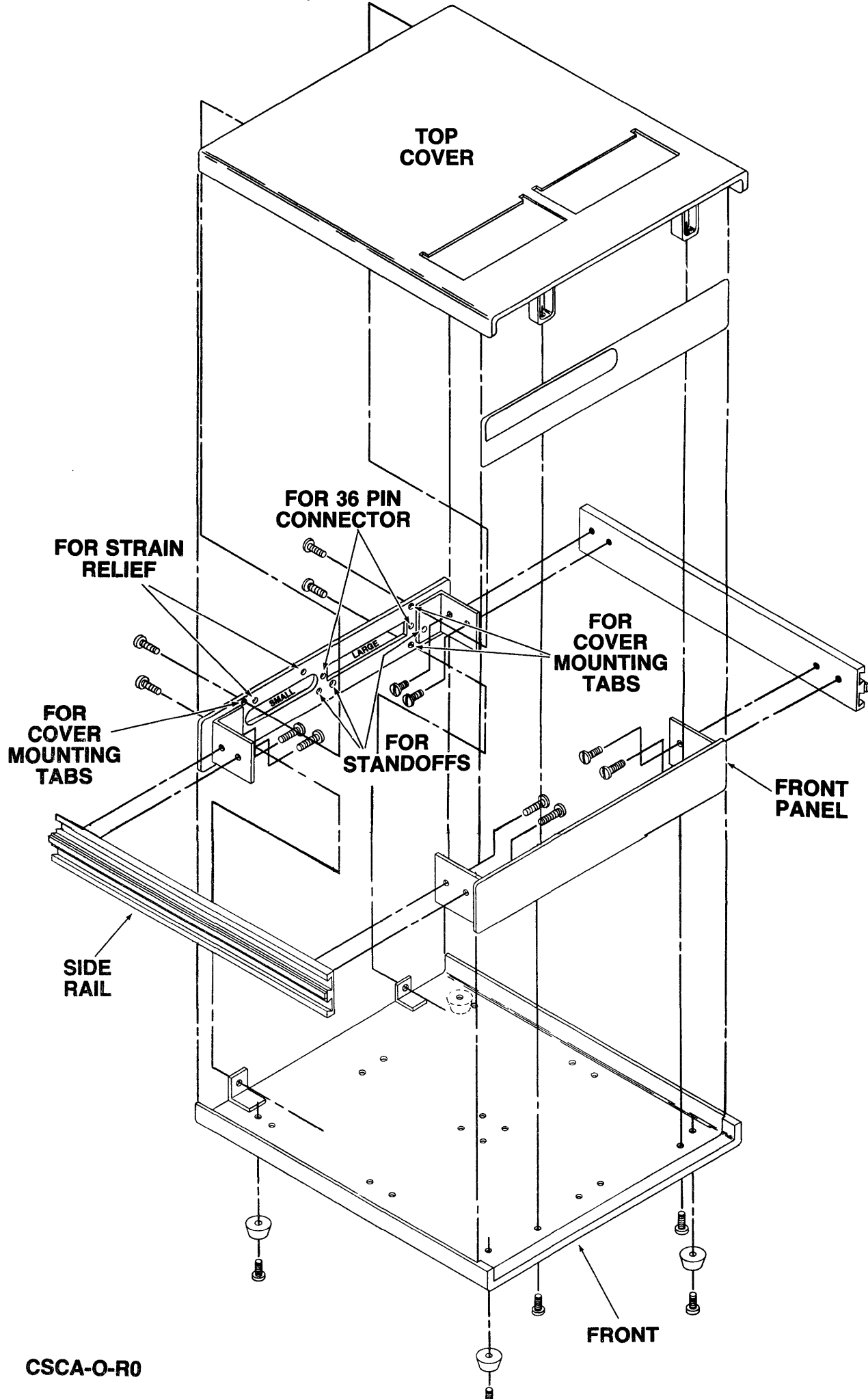
B. FRONT DRESS PANEL, REAR PANEL AND SIDE RAILS

1. Inspect the side rail and note that there is a small extension on each end. One extension is slightly longer than the other. THE END WITH THE LONGEST EXTENSION IS INTENDED TO GO TOWARD THE FRONT OF THE CABINET. After selecting the front end of each rail, attach each rail to the front and rear panels using eight 8-32x1/4" screws. The two outer-most holes on the rear panel are close to the bottom edge.
2. For two drive models without enclosed controller card and for four drive cabinet models, route the power and control wire cables down the side of the drives and out the round end slots provided in the rear panel.
3. Install the front/rear panel assembly on the lower cover with drives by setting the assembly down over the drives and into position in the lower cover. Pull excess cable through the rear panel. Screw the rear panel to the lower cover using the lower two holes on the rear panel that line up with the bracket on the lower cover. Attach using two 8-32x1/4" screws, no hex nuts required.

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C. UPPER COVER

1. Place the upper cover in place over the drives. This job is made easier by removing the plastic cassette cover (plastic door) which simply snaps out of the two hinges. Locate the cover over the drives and adjust the drives to center in the cutouts, then tighten the drive mounting screws.
2. Install two 8-32x1/4" screws through the rear panel at the upper two holes and lock the rear of the upper cover in place.
3. Install two 8-32x1/2" screws through two holes at the front of the cabinet bottom and lock the front of the upper cover in place. Do not over-tighten as these screws will not bottom out automatically. When they are snug, then STOP.



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